Recent Research Results

SAR ADC Algorithm with Redundancy

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Supported by STARC

Published in
T. Ogawa, H. Kobayashi, et. al.,
“SAR ADC Algorithm with Redundancy and Digital Error Correction”,
What is digital signal?

**Sampling**

**Quantization in time domain**

Take data • and discard the other data.
What is digital signal?

Quantization of Signal Level

Round the signal level to an integer.

Analog signal

Digital signal

Round the signal level to an integer.
Analog-to-Digital Conversion

(a) Analog Signal

(b) Sampling

(c) Quantization

(d) Quantization Noise

(e) Encoding
ADC is for Digital Signal Processing

Analog in real world

Digital In computer

SOC: System On a Chip

Sound
Temperature
Pressure
Video
Servo

INT
REF
ROM
RAM
CPU
TIMER
SCI
LOGIC
A/D
D/A
LOGIC
RAM
Outline

- Research purpose
- SAR ADC
- Binary search algorithm
- Non-binary search algorithm
- Proposed non-binary search algorithm
- DAC incomplete settling
- Conclusion
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Research purpose

• Automotive electronics is the spotlight now.
• High speed, reliable SAR ADCs in microcontroller are important there.
• Optimal digital error correction algorithm for their realization.
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• **SAR ADC**
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SAR ADC Block

SAR ADC is digital centric.

→ Suitable for fine CMOS implementation.
SAR ADC Characteristics

- High resolution (10-14bit)
- Middle sampling speed (10-40 MS/s)
- Small die area
- Low power (a few mW)
- Not use OP-amp
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Binary search algorithm

“Principle of a balance”

Vin = 4 - 1 = 3

Vin = 8 - 2 = 6

Comparison

Comparator output
Problem of binary search algorithm

No redundancy

Search result has error.

Digital output has error.
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Non-binary search algorithm
Non-binary search algorithm

Binary search algorithm (4-bit 4-step)

\[ D_{out} = 2^3 + 2^2 \cdot d_1 + 2 \cdot d_2 + 1 \cdot d_3 + 0.5 \cdot d_4 - 0.5 \]

Binary (Radix : 2)

Conventional non-binary search algorithm (4-bit 5-step)

\[ D_{out} = 2^3 + \gamma^3 \cdot d_1 + \gamma^2 \cdot d_2 + \gamma \cdot d_3 + 1 \cdot d_4 + 0.5 \cdot d_5 - 0.5 \]

Radix : \( \gamma \)

\[ \gamma = 2^{3/4} \]

\[ d_k : +1 \text{ or } -1 \]
Principle of error correction

Binary search algorithm

Comparator output: 1 0 0 1
Dout = 8 + 4 − 2 − 1 + 0.5 − 0.5 = 9

Non-binary search algorithm

Comparator output: 1 0 1 0 1
Dout = 8 + 3 − 2 + 1 − 1 + 0.5 − 0.5 = 9

Comparator output: 0 1 1 1 1
Dout = 8 − 3 + 2 + 1 + 1 + 0.5 − 0.5 = 9
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Proposed non-binary search algorithm

Conventional non-binary search algorithm

\[ D_{out} = 2^3 + \gamma^3 \cdot d_1 + \gamma^2 \cdot d_2 + \gamma \cdot d_3 + 1 \cdot d_4 + 0.5 \cdot d_5 - 0.5 \]

Radix: \( \gamma \)

\( \gamma = 2^{\frac{3}{4}} \)

Proposed Generalized non-binary search algorithm

\[ D_{out} = 2^3 + p_2 \cdot d_1 + p_3 \cdot d_2 + p_4 \cdot d_3 + p_5 \cdot d_4 + 0.5 \cdot d_5 - 0.5 \]

Flexible (not restricted to \( \gamma \))

Optimal design

\( d_k : +1 \) or \(-1\)
Design method of proposed algorithm

N-bit, M-step (M>N)

Design redundancy.

\[ 2^M - 2^N = \left( \sum_{i=1}^{M-1} 2^i q_i \right) \]

\( q_k \) : Redundancy at k-th step

Calculate step of reference voltage.

\[ p_{k+1} = -q_k + 2^{M-k-1} - \sum_{i=k+1}^{M-1} 2^{i-k-1} q_i \]

\( p_k \) : Step of reference voltage at k-th step
Proposed algorithm Example 1

Redundancy

Error

Correction

$q_1 = 2$

$q_3 = 1$

$q_2 = 1$

$p_2 = 3$

$p_3 = 2$

$p_4 = 1$

$p_5 = 1$
Proposed algorithm  Example 2

Redundancy

$q_1 = 4$
$q_2 = 2$

Error

$q_1 = 4$
$q_2 = 2$

Correction

$p_2 = 2$
$p_3 = 2$
$p_4 = 2$
$p_5 = 1$
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Settling of DAC output

Output of DAC [LSB]

Settling time [τ]

0 1 2 3 4 5

1/2LSB

Last step
First step

Short
Long
Conversion time of each algorithm

Binary search algorithm

Step 1 | Step 2 | Step 3 | Step 4

Exact DAC settling $\rightarrow$ Long time

Non-binary search algorithm

Step 1 | Step 2 | Step 3 | Step 4 | Step 5 | Step 6

Correct incomplete settling error.

Incomplete DAC settling $\rightarrow$ Short time
Simulation of AD Conversion Time

Binary algorithm
14-bit, 14-step
Step time: $9.1 \tau$

Proposed algorithm
14-bit, 22-step
Step time: $1.2 \tau$

Graph showing A/D conversion time with output of DAC (LSB) versus time. The graph compares the response of the Binary algorithm (red) and the Proposed algorithm (blue) with different step times.
Comparison of ADC speed

Conversion time of each algorithm (14-bit)

- Binary algorithm
- Conventional non-binary algorithm
- Proposed non-binary algorithm

Proposed algorithm: 20% faster
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Conclusion

SAR ADC for automotive

• Generalized non-binary algorithm.
• Optimal redundancy design method.
  → Reliable, Faster SAR ADC
• Digital Error Correction
  → Suitable for fine CMOS implementation.

20% faster than conventional non-binary algorithm only with ROM contents modification.
Non-Binary SAR ADC
Implementation and Measurement Results

0.18um CMOS
2.5mm x 2.5mm
with two SAR ADCs

SNDR comparison of
10step (binary) and 12step (non-binary)
$F_{in}$: 100kHz
Lesson from 老子

Redundancy makes ADC perform better

「無用」之「用」

Un-useful things are actually useful.