Typical n-MOSFET Modeling using A Skewing Method
— An n-MOSFET Modeling Method for RF Analog Circuit Design Centering—

Hitoshi AOKI† and Haruo KOBAYASHI†

†Faculty of Science and Technology, Division of Electronics and Informatics, Gunma University 1-5-1 Tenjin-cho, Kiryu, Gunma 376-8515, Japan
E-mail: †haoki@ieee.org

Abstract This paper presents a theoretical yet practical device targeting method to extract typical model parameters of MOSFET devices on wafer for RF analog integrated circuit design. This method employs skewing algorithms with existing model parameters of typical-like device which is selected by using inter-lot process electrical test parameters. To demonstrate the plausibility of this method a cascade amplifier is designed to simulate frequency characteristic of $S_{11}$ by using this method.

Keyword Statistical Modeling, RF-CMOS, Device Targeting, Typical Skewing, Process Test

1. Introduction
In order to design new analog integrated circuits in Engineering Design Automation (EDA) environment, SPICE model libraries of devices are important. The first step to develop model libraries in most semiconductor manufactures is to define the typical devices for model parameter extractions. Next step is to extract nominal model parameters [1] with DC current versus voltage (IV), capacitance versus voltage (CV), and S-parameters (only for RF) measurements by using any model parameter extraction software. After that, statistical model libraries are fabricated based on the typical model parameters. Statistical model libraries are used for reproducing device parameter distributions for yield simulations. However, their center value, which is typical, is mostly inaccurate. Conventional methods to define typical target specification are based only on process specifications and conditions without using test results of fabricated devices.

To define the typical specifications, which are the typical device characteristics of the true center device, is the key for circuit designers because the typical model dominates initial circuit design. Furthermore, it dominates next design step which is worst/best case simulations.

There are many papers such as [2]-[5] describing statistical modeling published in two decades. However, we could not find any papers which discussed typical device targeting for model extractions so far.

The proposed method is based on On-wafer process parametric electrical test (E-Test) [6] parameters. The test algorithms of DC and capacitances are customized and added to represent analog and RF characteristics. To calculate typical E-test parameters while maintaining parameter correlations, statistical functions including Probability Distribution Function (PDF), Skewness, and regression test are employed. Based on the calculated typical E-Test parameters, ‘typical-like’ device whose E-Test parameter values are as close as calculated typical are selected. After extracting model parameters of the selected ‘typical-like’ device, some of these model parameters are further skewed to the calculated typical E-Test parameters.

To confirm the plausibility of the proposed method, typical simulation results with a foundry library and with a library using the proposed method are compared by referring measured distributed characteristics. The results show the proposed method is much more accurate than a conventional method which a foundry used.

2. Procedure of The Proposed Targeting Method
In this research a flow (see Fig. 1) and the procedure of proposed typical targeting are described as follows;

1-4. DC and capacitance E-test algorithms are reviewed and added to the existing process tests while analyzing correlations between E-Test parameters and RF characteristics. Using the developed E-Test algorithms, recent 60 wafers in three lots are tested and stored in a database.

5-6. Target E-Test parameters are calculated with statistical analysis.

7. Then, the closest possible chip to the calculated E-Test parameters is found. If the closest chip was gone for production or other purposes, next closest possible chip could be selected. The selected chip/device is named as ‘typical-like’ device.

8-10. Using the ‘typical-like’ device the full model parameter set is extracted from DC, CV, and S-parameter measurements.
3. Calculations of Theoretical Target Specifications

3.1. Development of E-Test Parameters

E-Test parameters and their algorithms for calculating target specifications are modified by adding new functions to those which are generally used for Process Control Monitor (PCM) at any semiconductor manufacturers. However, test algorithms to obtain E-Test parameters must be clearly stated since some parameters will be used for skewing of model parameters.

DC E-Test parameters, including $TOX$, $DL$, $DW$, $Idsat$, $Gmmax$, $Beta$, $Rcon$, $Rdiff$, and $VT0$ are mainly used for PCM. The meanings of these parameters are listed in Table 3.

Since the first-order variables of the DC drain current equations in any MOSFET compact models consist of these parameters, we have reviewed and developed the test algorithms that are also used for SPICE model parameter extractions.

Since we focus on analog RF circuits, AC parameters have to be included. The KAIST’s small signal equivalent circuit [7] of an RF n-MOSFET (see Fig. 3) has been applied for the circuit analysis with complex $Y$-parameters, which can be easily converted to/from $S$-parameters. To observe the relationship between small signal circuit components and $Y$-parameters KAIST’s [7] analysis model is referred as

\begin{align}
Y_{11} &= \frac{j\omega (C_{gs} + C_{gd})}{1 + j\omega (C_{gs} + C_{gd})R_g} \\
Y_{12} &= \frac{-j\omega C_{gd}}{1 + j\omega (C_{gs} + C_{gd})R_g}
\end{align}

(1)

(2)
Table 1. E-Test parameters used for typical device targeting. Where, “Large” has maximum gate length (10.0 μm) and width (10.0 μm), “Narrow” has maximum gate length with minimum gate width (0.25 μm), and “Short” has minimum gate length (0.18 μm) with maximum gate width, respectively.

<table>
<thead>
<tr>
<th>E-Test Parameter</th>
<th>Test Definition</th>
<th>Device Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>TOX (Oxide thickness)</td>
<td>Maximum capacitance of $C_{gs}$ vs. $V_{sat}$</td>
<td>Large gate capacitance</td>
</tr>
<tr>
<td>LD (Diffusion length)</td>
<td>Shift and Ratio Method [8]</td>
<td>Large, Short</td>
</tr>
<tr>
<td>WD (Diffusion width)</td>
<td>Conventional Method [9]</td>
<td>Large, Narrow</td>
</tr>
<tr>
<td>Idsat (Saturation current)</td>
<td>Maximum drain current at $V_{gs}=0$ [V], $V_{ds}=V_{th}$</td>
<td>Large</td>
</tr>
<tr>
<td>$\Gamma_{m}$max (Maximum conductance)</td>
<td>Maximum trans-conductance at $V_{gs}=0$ [V], $V_{ds}=V_{th}$</td>
<td>Large</td>
</tr>
<tr>
<td>Beta</td>
<td>Medium Slope of $I_{ds}$ vs. $V_{gs}$ curve</td>
<td>Large, Narrow, Short</td>
</tr>
<tr>
<td>Reon (Contact resistance)</td>
<td>Contact resistance (Backend test [10])</td>
<td>Dedicated TEG [10]</td>
</tr>
<tr>
<td>Rdif (Diffusion resistance)</td>
<td>Diffusion resistance (Backend test [10])</td>
<td>Dedicated TEG [10]</td>
</tr>
<tr>
<td>VTO (Threshold voltage)</td>
<td>Conventional Method [10]</td>
<td>Large</td>
</tr>
<tr>
<td>COV (Overlap capacitance)</td>
<td>Overlap capacitance at $V_{gs} = V_{th}$ of $C_{gs}$ vs. $V_{gs}$ Curve</td>
<td>Large area (100μm x 100μm)</td>
</tr>
<tr>
<td>CJ (Area Junction capacitance)</td>
<td>Bulk-to-drain junction capacitance at $V_{j}=0$ [V]</td>
<td>Junction area &gt;&gt; Side-wall perimeter</td>
</tr>
<tr>
<td>CJW (Perimeter Junction capacitance)</td>
<td>Bulk-to-drain side-wall junction capacitance at $V_{j}=0$ [V]</td>
<td>Side-wall perimeter &gt;&gt; Junction area</td>
</tr>
</tbody>
</table>

\[
Y_{21} = \frac{g_m - j\omega C_m - j\omega C_{gd}}{1 + j\omega (C_{gs} + C_{gd}) R_g} 
\]

Where, gate-to-source ($C_{gs}$) and gate-to-drain ($C_{gd}$) capacitances include channel and overlap capacitances. For junction capacitances, only the bulk-to-drain junction capacitance ($C_{jd}$) is remained when the intrinsic body note is short-circuited to the source directly. $C_m$ is the trans-capacitance which representing the different effect of the gate and the drain on each other in terms of charging currents, just as $g_m$ is a trans-conductance representing the different effect of these two terminals on each other in terms of transport currents.

Parameters with underlines in equations (1) through (4) can be tested in E-Test. Unfortunately, gate resistance ($R_g$), substrate resistance under drain area ($R_{subd}$), and source-to-drain capacitance ($C_{sd}$) cannot be tested without using a network analyzer. However, the correlation analysis between $Y$-parameters and E-Test parameters can be made without $R_g$, $R_{subd}$, and $C_{sd}$.

The E-Test parameters and their test algorithms that we developed [1], [11]-[13] are shown in table 1. Especially for RF characteristics, $COV$ is correlated with $C_{gs}$, $C_{gd}$, and $C_m$. $CI$ and $CJW$ are correlated with $C_{jd}$. $Idsat$ is correlated with $g_m$, and $\Gamma_{m}$max and $Beta$ are correlated with $g_m$.

All of these E-Test parameters are not only used for calculation of target E-Test parameters but also for skewing target or extractions of common model parameters to be skewed.

3.2. Statistical analysis for typical parameter calculations

Using a control chart, typical lot/wafers are selected for typical targeting analysis and modeling such as shown in Fig. 4. E-Test parameters that we adopted to avoid any conflicts are $LD$, $VTO$, and $TOX$.

Outliers of any data points should be neglected by using PDF plots as shown in Fig. 5. All E-Test parameters other than $VTO$ and $ldsat$ need to be screened. However, Skewness [14], which is a statistical function to characterize the degree of asymmetry around its mean, has been programed for automations. The equation is written as
Fig. 4 Lot/Wafer screening with a control chart. In addition to LD, VT0 and TOX have been analyzed for selecting typical lot/wafer.

Fig. 5 PDF for E-Test parameters of n-MOSFETs, (a) VT0 for Large device, (b) Idsat for Short device. For both graphs, horizontal axis is the frequency (counts) and vertical axis is the value of each parameter.

Fig. 6 An instance of the correlation matrix of E-Test parameters. Since the matrix is symmetrical, correlation numbers are plotted in the upper area and 2-D raw data distribution is plotted in the lower area. Where, numbers surrounded by red colored bold frames are two parameters that have strong correlations.

\[
\text{Skewness} = \frac{1}{N} \sum_{j=1}^{N} \left( \frac{x_j - \bar{x}}{\sigma} \right)^3
\] ................................................................. (5)

Where \(\sigma\) is the standard deviation, \(N\) is the number of samples, \(x_j\) is the parameter value, \(\bar{x}\) is the mean.

A positive value of Skewness signifies a distribution with an asymmetric tail extending out towards more positive \(x\); a negative value signifies a distribution whose tail extends out towards more negative \(x\). Using the result outlier data points are neglected. After all, the mean value of each E-Test parameter is calculated.

As shown in Fig. 6, some pairs of E-Test parameters have strong correlations whose absolute value of correlation factor should be more than or equal to 0.6 [15]. These correlations must be kept for calculating typical E-Test parameters in order to avoid the calculation of unrealistic parameter combinations. The regression test [14] is employed to check the parameter correlations.

4. Target Device Selection and Its Modeling

Using the calculated typical E-Test parameters in chapter 3, an existing device which has the closest specifications is picked up. The device can be used for full model parameter extractions. The device is called as a ‘typical-like’ device. The typical E-Test parameters and the selected ‘typical-like’ device name are listed in Fig. 7 by using our program which is implemented into statistical modeling software (MOSTAT™ [16]).

For the purpose of statistical modeling, the MOSFET model must be physical and is compatible with RF and analog simulations. Since the physical parameters need to maintain process properties, these parameters should be extracted by numerical methods without optimizations. In this research we selected BSIM4 as a deep sub-micron MOSFET model. Full model parameter extractions of the typical-like device are carefully and accurately performed with DC, CV, and S-parameter measurements.

5. Model Parameter Skew to the Typical E-Test Parameters

The physical parameters of the extracted BSIM4 model parameters [15], [17] of the ‘typical-like’ device need to be selected under the following conditions;

(エラー！参照元が見つかりません。) The model parameters are physical and process oriented.

(エラー！参照元が見つかりません。) The slope of IV or CV should not be changed
By referring the model equations, E-Test parameters, which will be the skew targets, are carefully chosen. In our research physical model parameters that we selected for skewing are listed in Table 2.

As shown in Figs. 8 and 9, all simulated curves should be monitored simultaneously to avoid inconsistency during each skewing procedure in DC and CV. After the skewing procedure, all simulation curves with skewed parameters for skewing.

Table 2: E-Test parameters for target and BSIM4 model parameters for skew.

<table>
<thead>
<tr>
<th>Type of the simulation</th>
<th>E-Test parameter as targets</th>
<th>BSIM4 Model parameters for skewing</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ids vs. VGS (Large device)</td>
<td>VT0.Large</td>
<td>VTH0</td>
</tr>
<tr>
<td>g_m vs. VGS (Large device)</td>
<td>GMMAX.Large, BETA.Large</td>
<td>UA</td>
</tr>
<tr>
<td>Ids vs. VGS (Narrow device)</td>
<td>VT0.Narrow</td>
<td>K3, WINT, DVT0W</td>
</tr>
<tr>
<td>Ids vs. VDS (Large device)</td>
<td>Idsat.Large</td>
<td>U0</td>
</tr>
<tr>
<td>Ids vs. VDS (Narrow device)</td>
<td>Idsat.Narrow</td>
<td>WINT</td>
</tr>
<tr>
<td>C_GC vs. V_GC</td>
<td>COV</td>
<td>CGS0 (=CGD0), CGSL (=CGDL)</td>
</tr>
<tr>
<td>C_J vs. V_J (Area &gt;&gt; Perim.)</td>
<td>C_J.area</td>
<td>C_J0</td>
</tr>
<tr>
<td>C_J vs. V_J (Area &lt;&lt; Perim.)</td>
<td>C_J.perim</td>
<td>CJSW</td>
</tr>
</tbody>
</table>

Fig. 7 Typical E-Test parameters and a typical-like device selection with MOSTAT™.

Fig. 8 Model parameter skewing CV plots. A dot in each plot is the E-Test parameter target value. Two CV plots show simulations of the ‘typical-like’ device and final (skewed) model parameters. (a) is the gate capacitance and (b) is the area junction capacitance respectively.

Fig. 9 Typical E-Test parameters and a typical-like device selection with MOSTAT™.
Fig. 9 Model parameter skewing DC plots. A dot in each plot is the target E-Test parameter value. All of seven DC plots show simulation results of the ‘typical-like’ device and final (skewed) model parameters. (a), (b), and (c) are the log ($I_{ds}$) vs. $V_{gs}$ at $V_{ds}=50$ [mV] and $V_{bs}=0$ [V], $g_m$ vs. $V_{gs}$ at $V_{ds}=50$ [mV] and $V_{bs}=0$ [V], and $I_{ds}$, $V_{ds}$ at $V_{gs}=$VDD and $V_{bs}=0$ [V], all for Large device, respectively. Then, (d) and (e) are the log ($I_{ds}$) vs. $V_{gs}$ at $V_{ds}=50$ [mV] and $V_{bs}=0$ [V] and $I_{ds}$, $V_{ds}$ at $V_{gs}=$VDD and $V_{bs}=0$ [V], all for Narrow device, respectively. (f) and (g) are the log ($I_{ds}$) vs. $V_{gs}$ at $V_{ds}=50$ [mV] and $V_{bs}=0$ [V] and $I_{ds}$, $V_{ds}$ at $V_{gs}=$VDD and $V_{bs}=0$ [V], all for Short device, respectively.

In each plot is located on lower side and the upper side curve in each plot is the simulation before skew.

6. Verifications of RF Circuit Simulations

Entire procedure of the typical skewing has been implemented into MOSTAT™ with C/C++ languages. Especially for the typical skew, it is very difficult to obtain correct results without any software tools.

In order to verify proposed typical targeting method, the cascode amplifier designed in Fig. 2 has been simulated by using skewed typical BSIM4 parameters. Because of our limited resources, only the magnitude of $S_{21}$ could be measured. The simulated curve is labeled as “Proposed RF Typical” in Fig. 10. To evaluate the accuracy of our skewing procedure, we prepared ‘most typical’ device whose E-Test parameters are much closer to the typical target values than ‘typical-like’ device values. As shown in Fig. 10, the skewed results of “Proposed RF Typical” are very close to ‘most typical’ device. Moreover, our “Proposed RF Typical” curve is located in the middle of 100 $S_{21}$ curves which we measured, whereas the typical data simulated with a model supplied by a foundry is far from the center. Also, the $S_{21}$ slope of proposed typical model is consistent with measured data.

7. Conclusions

A new procedure of n-MOSFET typical target and a skewing method for RF analog applications were demonstrated. For the experiments, 0.18 μm RF CMOS process devices, whose oxide thickness was 4.2 nm, were employed. A simple cascode amplifier was designed and fabricated in our TEG in order to verify n-MOSFET typical targeting results.

The skewed results were very close to “most typical device.” Moreover, our “Proposed RF Typical” curve is located in the middle of 100 $S_{21}$ curves which we measured, whereas the typical data simulated with a model supplied by a foundry is far from the center. This typical model generation method is practical. Therefore, it is useful for any CMOS circuit designers.

We will enhance this method to corner/boundary and mismatch modeling to complete total statistical modeling procedure.
Fig. 10 Measurement and simulation results of $S_{21}$ dependencies on frequency of the cascode amplifier (Fig. 2). The center solid line is the simulation with proposed typical BSIM4 parameters, and the solid line below is the simulation with typical BSIM4 parameters supplied by a foundry. A hundred of break lines are measured $S_{21}$ of randomly selected MOSFETs that were from the recent 60 wafers in three lots.

References


[16] MOSTAT\textsuperscript{TM}, http://www.modech.co.jp/