Time-to-Digital Converter Architecture with Residue Arithmetic and its FPGA Implementation

Congbing Li    Kentaroh Katoh
Junshan Wang   Shu Wu
Shaiful Nizam Mohyar   Haruo Kobayashi

Gunma University
Tsuruoka National College of Technology
Outline

• Research Objective & Background
• Flash TDC and Problems
• Residue Arithmetic TDC Architecture
• FPGA Implementation
• Conclusion and Future Work
Outline

• Research Objective & Background
  • Flash TDC and Problems
  • Residue Arithmetic TDC Architecture
  • FPGA Implementation
• Conclusion and Future Work
Research Objective

Objective

● Development of Time-to-Digital Converter (TDC) architecture with high-speed and small hardware

Approach

● Utilization of residue arithmetic
  Signal is “time” instead of “voltage”
  Residue can be easily obtained with ring oscillator.
Research Background

TDC plays an important role in nano-CMOS era

Voltage-domain resolution facing difficulties due to reduced supply voltage

Time-domain resolution becoming superior

TDC measures time interval between two signal transitions, into digital signal.
(widely used in ADPLLs, jitter measurements, time-domain ADC)
Outline

• Research Objective & Background
• Flash TDC and Problems
• Residue Arithmetic TDC Architecture
• FPGA Implementation
• Conclusion and Future Work
Flash TDC

- Digital output (Dout) proportional to time difference between rising edges (T)

- Time resolution $\tau$
Problems of Flash TDC

An n-bit flash TDC with \(2^n\)-quantization levels

Advantages
- High-speed timing measurement
- Single-event timing measurement
- All digital implementation

Disadvantages
- \(2^n-1\) delay elements, \(2^n-1\) Flip-Flops
- n-bit thermometer-to-binary code encoder

\[\text{Large circuits} \]
\[\text{High power consumption}\]
Outline

• Research Objective & Background
• Flash TDC and Problems
• Residue Arithmetic TDC Architecture
• FPGA Implementation
• Conclusion and Future Work
Residue Arithmetic

\( m_1, \ldots, m_r \) are positive integers and coprime each other then there is a unique positive integer \( x \) for given integers \( (a_1, \ldots, a_r) \) can satisfy the following:

\[ x \equiv a_k \pmod{m_k}, \quad k = 1, 2, \ldots, r \]

where \( 0 \leq a_k < m_k \), \( 0 \leq x < N \) \((N = m_1 \cdot m_2 \cdots m_r)\).

Example

\( m_1 = 2, m_2 = 3, m_3 = 5 \)

\( N = 2 \times 3 \times 5 = 30 \)

each \( K \) is mapped to residues of \((m_1, m_2, m_3)\) one to one.

Table 1. An integer \( k \) and residues of \((m_1, m_2, m_3)\)
Residue Arithmetic TDC Architecture

For TDC, signal is “time” instead of “voltage.”

Residue can be easily obtained with ring oscillator.

Example

Three ring oscillators, with delay of $2\tau$, $3\tau$, $5\tau$ respectively.

Then the elapsed time $T$ from oscillation can be obtained as:

- When $T \equiv a \pmod{2\tau}$,
- $\equiv b \pmod{3\tau}$,
- $\equiv c \pmod{5\tau}$,

and $K$ equals residues of $(a, b, c)$

$T = K \times \tau$
Proposed TDC
m1=2, m2=3, m3=5
N=2*3*5=30
the residues a(mod 2), b(mod 3), c(mod 5) are obtained with ring oscillators

Proposed TDC vs. Flash TDC

<table>
<thead>
<tr>
<th></th>
<th>Flash TDC</th>
<th>Proposed TDC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of delay elements</td>
<td>N = 2<em>3</em>5=30</td>
<td>M=2+3+5=10</td>
</tr>
<tr>
<td>Number of Flip-flop</td>
<td>N =2<em>3</em>5=30</td>
<td>M=2+3+5=10</td>
</tr>
</tbody>
</table>

Fig 4. Residue Arithmetic TDC Architecture
Outline

• Research Objective & Background
• Flash TDC and Problems
• Residue Arithmetic TDC Architecture
• FPGA Implementation
• Conclusion and Future Work
Proposed residue arithmetic TDC is implemented on Xilinx FPGA

Fig 5. Proposed TDC implementation on FPGA
Table 2. Measurement results of the proposed TDC

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0.00</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>30.30</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>6</td>
<td>60.60</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>2</td>
</tr>
<tr>
<td>9</td>
<td>90.90</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>12</td>
<td>121.20</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>4</td>
</tr>
<tr>
<td>15</td>
<td>151.50</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>5</td>
</tr>
<tr>
<td>18</td>
<td>181.80</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>6</td>
</tr>
<tr>
<td>21</td>
<td>212.10</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>7</td>
</tr>
<tr>
<td>24</td>
<td>242.40</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>8</td>
</tr>
<tr>
<td>27</td>
<td>272.70</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>9</td>
</tr>
<tr>
<td>30</td>
<td>303.00</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>10</td>
</tr>
<tr>
<td>33</td>
<td>333.30</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>11</td>
</tr>
<tr>
<td>36</td>
<td>363.60</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>12</td>
</tr>
<tr>
<td>39</td>
<td>393.90</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>13</td>
</tr>
<tr>
<td>42</td>
<td>424.20</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>14</td>
</tr>
<tr>
<td>45</td>
<td>454.50</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>15</td>
</tr>
<tr>
<td>48</td>
<td>484.80</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>16</td>
</tr>
<tr>
<td>51</td>
<td>515.10</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>17</td>
</tr>
<tr>
<td>54</td>
<td>545.40</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>18</td>
</tr>
<tr>
<td>57</td>
<td>575.70</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>19</td>
</tr>
<tr>
<td>60</td>
<td>606.00</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>20</td>
</tr>
<tr>
<td>63</td>
<td>636.30</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>21</td>
</tr>
<tr>
<td>66</td>
<td>666.60</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>22</td>
</tr>
<tr>
<td>69</td>
<td>696.90</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>23</td>
</tr>
<tr>
<td>72</td>
<td>727.20</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>24</td>
</tr>
<tr>
<td>75</td>
<td>757.50</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>25</td>
</tr>
</tbody>
</table>
The value of $K$

Time between rising edges of START and STOP signals (ns)

Fig 6. Measurement results of the proposed TDC
Outline

• Research Objective & Background
• Flash TDC and Problems
• Residue Arithmetic TDC Architecture
• FPGA Implementation
• Conclusion and Future Work
Conclusion and Future Work (1/2)

Proposed TDC vs. Flash-type TDC in general

<table>
<thead>
<tr>
<th></th>
<th>Flash TDC</th>
<th>Proposed TDC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of delay elements</td>
<td>$N = m_1 \cdot m_2 \cdots m_r$</td>
<td>$M = m_1 + m_2 + \cdots + m_r$</td>
</tr>
<tr>
<td>Number of Flip-flop</td>
<td>$N = m_1 \cdot m_2 \cdots m_r$</td>
<td>$M = m_1 + m_2 + \cdots + m_r$</td>
</tr>
</tbody>
</table>

the power consumption and chip size can be reduced significantly when $M << N$

the measurement errors caused by the delay element mismatch and flip-flop metastability can be reduced
Proposed TDC can be implemented on FPGA. The measurement results verify the operation principle by adapting the number of delay cells and Flip-flops, proposed TDC can be applied to any given sequence of integers.

Future work
Evaluate the measurement error when three ring oscillators have deviations in characteristics.

We acknowledge STARC for their kind support.
Q1: START and STOP signal are connected to user push bottoms, then how can you control the timing?

Q2: Interesting idea. Now this idea is implemented on FPGA, will you implement this in Silicon CMOS?

Q3: There are several TDC topologies. In your proposed design, what is the main focus?

Q4: Are there any drawbacks for this TDC design?
ISOCC Pictures