Linearity Improvement Algorithm for Current Steering DAC Based on 3-Stage Sorting of Half-Unary Current Sources

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Mismatch among current sources is one of dominant sources of nonlinearity for current-steering digital to analog converters (DACs) (Figs.1, 2); it deteriorates both static and dynamic DAC performance, and the reduction of the current source mismatch effects is important. Previous works have shown that its effects can be reduced by proper mapping or calibration techniques.

In this paper, we propose a half-unary current steering DAC with a current source sorting algorithm as calibration technique to deal with the current source mismatch that generates inside the mirrored current source structure. The half-unary structure is used to improve the differential non-linearity (DNL) while the current source sorting technique for integral non-linearity (INL) improvement (Figs. 3, 4).

Our MATLAB simulation shows in Fig.5 that by reducing the effect of current source mismatches, better suriprous free dynamic range (SFDR) is achieved. In additional, the second and third order harmonic distortions are also successfully suppressed. The comparison has been done with a 12-bit conventional unary, 12-bit unary and half-unary with 2-stage current sorting in case that the static current source mismatches are considered.

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