A Practical BIST Circuit for Analog Portion in Deep Sub-Micron CMOS System LSI

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Contents of Presentation

• Research background
• New architecture of analog BIST & LSI tester
• Simulation results of the proposed architecture
• Conclusion
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Research Background

• System LSI testing becomes more difficult
due to its analog portion.

• BIST for **Digital** : Successful (memory BIST, SCAN)
• BIST for **Analog** : Doubtful!

• **BIST**: Built-In-Self-Test

• **Digital** Test : Functionality **Easy!**
• **Analog** Test : Functionality & **Quality** **Hard!**
Discussion on Analog BIST

• Contradiction of analog BIST
  • Goodness of BIST in DUT should be assumed.
• Analog BIST must be simple
  • Failure rate of BIST $\ll$ Failure rate of whole DUT
  • BIST IP should survive against CMOS scaling

Analog BIST should be supported by LSI tester.
Target Performance

• To measure >1GHz signal with >10bit accuracy
• at low cost, for system LSI testing.

• Assumption
• LSI tester
• - provides repetitive signals to DUT
• - generates DC signals
• - controls every timing of digital portion.
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System Level Consideration

[Conventional Way]
DUT

1GHz, >10bit

Cable Problem

Cost: High

LSI Tester
T/H

ADC

[Sampler in DUT]
DUT

T/H

1kHz, >10bit

Hard to Design
1GHz, >10bit

Cost: Low

LSI Tester
ADC
Proposed Way

This works as a modified SA ADC.
Conventional SA ADC

SA: Successive Approximation

- **T/H circuit** holds the input signal.
- Its output is compared with $V_{DAC2}$.
- **T/H circuit**: high-speed, high-accuracy
- **Input signal**: non-repetitive as well as repetitive
Track and Hold Operations

(Hold during conversion) almost = (Sample in same phase)

repetitive waveform
Proposed SA ADC

- Repetitive input signal $V_{in}$ is compared with $V_{DAC}$.
- Its result is held by a latch.

Realized in LSI Tester
only High-Accuracy

Built in DUT
only High-Speed

• Repetitive input signal $V_{in}$ is compared with $V_{DAC}$.
• Its result is held by a latch.
Waveform Reconstruction by Equivalent-Time Sampling

- Repetitive signal waveform reconstruction
- from measured points in different phases.
Optional Concept for Proposed BIST

• As the conversion process goes on,
  • $V_{DAC2}$ approaches the held voltage.

「Diff Amp」 works as an amplifier.
CMOS T/H Circuit Linearity Consideration

• >10bit T/H circuit
• with deep submicron CMOS difficult to design

• Proposed architecture
• DC DAC: Upper 4-5 bit
• CMOS T/H : lower 5-7bit easy to design
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Simulation Results: Comparator2

\[ f_{in} = 1\text{GHz}, \quad f_{CLK} = 100.123\text{MHz} \]
Simulation Results: Master/Save-type T/H

*** Master/Slave T/H Circuit ***

- Clock
- Vout-master
- Vout-buffer-p
- Vin
- Vout-buffer-n
- Vout-slave
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Conclusion

• New architecture of analog BIST
  - to measure >1GHz signal with >10bit accuracy from system LSI.
  - supported by LSI tester.
  - simple, fast but low-accuracy circuits in DUT.
  - accurate but slow circuits in LSI testers.
  - it can cover fine CMOS.

• This analog BIST is applicable
  for our commercial LSI test systems.
Conversion Error caused by Noise  
Under investigation

• Assumption: Right answer of AD conversion is “1000”

• If the conversion result of MSB is “0” by the effect of noise,
• It is impossible to compensate this miss-conversion

The result of conversion through whole process must be “0111”