Design of Hysteresis Controlled Single-Inductor Multi-Output DC-DC Converter

Shunsuke Tanaka¹ *, Tatsunori Nagashima¹, Yasunori Kobori¹, Kotaro Kaneya¹, Takashi Okada¹, Takahiro Sakai¹, Biswas Sumit Kumar¹, Nobukazu Takai¹, Haruo Kobayashi¹
¹Gunma University 1-5-1 Tenjin-cho, Kiryu 376-8515, Japan
*t13801462@gunma-u.ac.jp ; takai@gunma-u.ac.jp

Nowadays, various applications require DC-DC converters with multiple output voltages. DC-DC converters are desirable for small size and low cost. To overcome this problem, single-inductor multiple-output (SIMO) converters have recently been introduced [1],[2]. However they suffer from performance degradation with conventional control methods because the energy charged in one inductor is distributed to each output voltage one by one.

In this paper, we study a hysteresis control method applied to single-inductor dual-output (SIDO) converters, which can obtain faster response and lower voltage ripple. As shown in Fig.1, compared with current controlled PWM converter, the proposed hysteresis controlled converter does not require saw-tooth wave generator or current sensor.

First, we have evaluated the performance of single-inductor single-output (SISO) power supply circuit using the proposed hysteresis control with simulation and experiment. Next, we have applied the hysteresis control to SIDO power supply and verified its performance with simulation and experiment.

Furthermore, we propose a new SIDO circuit for the output voltage ripple reduction as shown in Fig. 2. In the proposed circuit, output voltages are set as Vo1 > Vo2. Timing chart for the proposed SIDO buck converter circuit operation is shown in Fig.3. In the timing chart, in mode 1 (when both S1 and S2 are off) the inductor current is charged but it is not supplied to Vo1, Vo2. In mode 2 (S1 is on, S2 is off) the inductor current is supplied to Vo1. Similarly in mode 3 (S1 is off, S2 is on) the inductor current is supplied to Vo2. In mode 4 (both S1, S2 are on), the inductor current is supplied to the lower voltage terminal, i.e., Vo2. Fig.4 shows the simulation results, and we see that the static output voltage ripple is less than 15mVpp and the transient voltage ripple is within 13mVpp.