Multi-bit Sigma-Delta TDC Architecture for Digital Signal Timing Measurement

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Outline

► Research Objective
► Single-Bit & Multi-Bit ΣΔ TDCs
► Multi-Bit ΣΔ TDC with DWA
► Multi-Bit ΣΔ TDC with Self-Calibration
► Circuit Design
► Conclusion
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Research Purpose

- Testing timing difference between two repetitive digital signals.
  Ex. Data and clock in Double Data Rate (DDR) memory

- Short testing time
- Good accuracy

Implemented with small circuitry
Our Work

Using Multi-bit $\Sigma\Delta$ Time-to-Digital Converter (TDC)

- Repetitive digital signals
  $\Sigma\Delta$ TDC can be used
- Simple circuit
- Fine time resolution

<table>
<thead>
<tr>
<th></th>
<th>Testing time</th>
<th>Linearity</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single-bit</td>
<td>Long</td>
<td>Good</td>
</tr>
<tr>
<td>Multi-bit</td>
<td>Short</td>
<td>Bad</td>
</tr>
</tbody>
</table>

due to delay elements mismatches

Two methods for their compensation
- Data-weighted-averaging (DWA)
- Self-calibration
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Single-Bit ΣΔ TDC

- Measurement of timing $T$ between repetitive CLK1 and CLK2.
- Number of 1’s at $D_{out}$ is proportional to $T$.
- Time resolution becomes finer as measurement time becomes longer.
Multi-Bit $\Sigma \Delta$ TDC

- 3-bit: $2^3 - 1 = 7$ comparators and delays
- Fine time resolution with a given measurement time

Shorter measurement time with a given time resolution

- TDC non-linearity due to mismatches among delay cells.
Multi-Bit ΣΔ TDC

- 3-bit: $2^3 - 1 = 7$ comparators and delays
- Fine time resolution with a given measurement time
- Shorter measurement time with a given time resolution
- TDC non-linearity due to mismatches among delay cells.
Multi-Bit ΣΔ TDC

- 3-bit: $2^3 - 1 = 7$ comparators and delays
- Fine time resolution with a given measurement time

\[ \text{Shorter measurement time with a given time resolution} \]

- TDC non-linearity due to mismatches among delay cells.
Multi-Bit $\Sigma\Delta$ TDC

- **3-bit**: $2^3 - 1 = 7$ comparators and delays
- Fine time resolution with a given measurement time

Shorter measurement time with a given time resolution

- TDC non-linearity due to mismatches among delay cells.
# Difference in Measurement Time

- **Simulation conditions**

<table>
<thead>
<tr>
<th></th>
<th>1-bit ΣΔ TDC</th>
<th>3-bit ΣΔ TDC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rising timing edge difference (T)</td>
<td>-0.9 ~ 0.9ns (Resolution : 0.04ns)</td>
<td>-0.9 ~ 0.9ns (Resolution : 0.04ns)</td>
</tr>
<tr>
<td>Delay time (τ)</td>
<td>1ns</td>
<td>0.145ns</td>
</tr>
<tr>
<td>The number of digital outputs</td>
<td>2</td>
<td>2</td>
</tr>
</tbody>
</table>

- **A rising number of outputs for the interval T**

✓ Multi-bit takes short measurement time for a given time resolution ⇒ Low cost
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DWA (Data Weighted Averaging)

- Flash ADC outputs shuffled by DWA logic, fed into MUXs as select signals

- Delay mismatch effects moved to high-frequency (noise-shaping)
Noise-Shaping

\[ Y(z) = X(z) + (1 - 1/Z)\Delta\tau(z) \]

Delay mismatch \( \Delta\tau \) is first-order noise-shaping.
DWA & Noise Shaping

- Delay $\tau$: integration & differentiation
- Delay mismatch $\Delta\tau$: differentiation

![Diagram of delay cell mismatch effects]

Without DWA:

With DWA:
DWA Operation

Passing a baton in relay race!
DWA Effect

- Delay $\tau$: integration & differentiation
- Delay mismatch $\Delta \tau$: differentiation

Measurement $T$

$T$ is DC signal.

Without DWA

With DWA

Mismatch effects reduction at DC
Simulation of $\Sigma\Delta$ TDC with DWA

- Output: 99 points
- Output: 599 points

- Reduce the effect of delay mismatches.
  - $\Sigma\Delta$ TDC linearity is improved.
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Self-calibration circuit: inverter, MUX, counter, memory

Measure delay values and store them in memory.
Self-Measurement of Delay

- Ring oscillator with a delay cell to be measured.
- Counter measure the number of the pulses.
- $\Delta \tau_1$ can be calculated.
- Measured delay values are stored in memory.
Time Signal & Ring Oscillator

Measurement: \( \tau + \Delta \tau_1 \)

Ring oscillator

Möbius strip
Self-Measurement of Delay

Measurement: $\tau + \Delta \tau_1$

Oscillation frequency

$$f = \frac{1}{2(\tau' + \tau + \Delta \tau_1)}$$

Measure $\Delta \tau_2, \Delta \tau_3, \Delta \tau_4, \ldots, \Delta \tau_N$ one by one.

$\Delta \tau_1$ can be calculated from the oscillation frequency
Essence of Proposed Method

- All operations are done in **digital domain**.
- Signal is **Time** instead of **Voltage**.

Easy, accurate measurement of $\Delta \tau$

Time flies like an arrow!
Proposed Error Correction Scheme

- Obtain TDC raw output ($D_{out}$) for two input clocks.
- Read delay values from memory, and compensate for the output based on them.
Simulation of Self-Calibration

- Output: 99 points

- Output: 599 points

ΣΔ TDC linearity is improved.
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Single-Bit ΣΔ TDC

Phase Frequency Detector

Charge Pump with Operational Amplifier

PFD + Integrator

Up

Down

Dout

clk
Multi-Bit ΣΔ TDC

Delay cell array
Circuit Design of Multi-Bit ΣΔ TDC

Array of comparators whose outputs are connected to MUX select signals.
Simple digital circuit:
Two Registers, Encoder, Adder, Barrel Shifter
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## Circuit Performance Comparison

<table>
<thead>
<tr>
<th></th>
<th>Flash TDC</th>
<th>1-bit $\Sigma\Delta$ TDC</th>
<th>Multi-Bit $\Sigma\Delta$ TDC (without correction)</th>
<th>Multi-Bit $\Sigma\Delta$ TDC (with correction)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Circuitry</td>
<td>😞 😞</td>
<td>😊</td>
<td>😊</td>
<td>😊</td>
</tr>
<tr>
<td>Resolution</td>
<td>😞 😞</td>
<td>😞</td>
<td>😊</td>
<td>😊</td>
</tr>
<tr>
<td>Accuracy</td>
<td>😞</td>
<td>😊</td>
<td>😞 😞</td>
<td>😊</td>
</tr>
<tr>
<td>Time</td>
<td>😊</td>
<td>😞</td>
<td>😊</td>
<td>😊</td>
</tr>
</tbody>
</table>
We propose to use $\Sigma\Delta$ TDC for digital signal timing measurement.

Multi-bit $\Sigma\Delta$ TDC.
- Short measurement time
- Fine time resolution.
- Non-linearity due to mismatches among delay cells.

Two techniques to improve linearity
- DWA
- Self-Calibration (signal is “time”)

Low cost, high quality digital timing test can be realized.
Appendix
• Arbitrary digital timing signals can be measured one input.
• Circuitry is large.
• Time resolution is $\tau$.

• Measured repetitive digital signals.
  ➢ High quality testing is required.

Arbitrary signals
  ➢ $T$ is changed.

Repetitive signals
  ➢ $T$ is constant.
How to Calculate the Delay Time

\[ f_{osc}^k \approx \frac{M_k}{T_{ref}} = \frac{1}{2(\tau' + \tau_k)} \]

\[ f_{osc}^0 \approx \frac{M_0}{T_{ref}} = \frac{1}{2\tau'} \]

\[ \tau_k = \frac{1}{2} \left( \frac{1}{f_k} - \frac{1}{f_0} \right) \approx \frac{T_{ref}}{2} \left( \frac{1}{M_k} - \frac{1}{M_0} \right) \quad \text{k=1, 2, \ldots, } 2^{N-1} \]
各遅延値に重みをもたせる
測定にはN-bit で Nステップかかる
Comparison of Linearity

- 3-bit ΔΣ TDC (Delay Time(Ideal) : \( \tau = 0.145\text{ns} \))

Output pulses : 99

- Ideal state : The error is from -2ps to +2ps.
- After calibration : The error is from -2.5ps to +2.5ps.
  - The linearity is improved.
シグマデルタ型TDC回路の動作①

- CLK1とCLK2を入力
- 比較器出力により経路選択
  ➢ CLK1a, CLK2aを得る
タイムジェネレータによりMask信号（=速い方の信号）を発生させる
- Mask信号とCLK1a, CLK2aとの論理積をとり、立下りを合わせる
- CLK1b, CLK2bを得る
シグマデルタ型TDC回路の動作③

- CLK1bとCLK2bとの差を取り結果のCLKינを積分
- 比較器でINT_outを0と比較し、出力D_outを得る
  ➢ 次のクロックでの経路を制御
タイミングチャート（$D_{out}=1$のとき）

CLK1

CLK2

CLK1a

CLK2a

Mask=CLK2a

CLK1b

CLK2b

$CLK_{in}$

$INT_{out}$

CK

$T_d$
タイミングチャート($D_{out}=0$のとき)

CLK1

CLK2

CLK1a

CLK2a

Mask=CLK1a

CLK1b

CLK2b

CLK_{in}

INT_{out}

CK

$T$

$\tau$

$T_d$