Fast Testing of Linearity and Comparator Error Tolerance of SAR ADCs

T. Ogawa, H. Kobayashi, S. Uemori, Y. Tan, S. Ito, N. Takai, T.J. Yamaguchi

Gunma University
Outline

• Research purpose
• SAR ADC
• Fast testing of SAR ADC DC linearity
• Testing of comparator-error tolerance in non-binary SAR ADC
• Conclusion
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Research purpose

- Successive Approximation Register (SAR) ADCs
  - Widely used
  - low sampling rate, high resolution
  - Testing time is long → Costly

- BIST for fast DC linearity testing
- BIST for SAR ADC redundancy check in cooperation with ATE

ATE : Automatic Test Equipment
BIST : Built-In-Self -Test
Outline

• Research purpose
• **SAR ADC**
  • Fast testing of SAR ADC DC linearity
  • Testing of comparator-error tolerance in non-binary SAR ADC
• Conclusion
SAR ADC is digital centric.

→ Suitable for fine CMOS implementation.

• Small chip area
• Low power
• Not use OP-amp
**SAR ADC Principle Operation**

- **Binary search case**

**4bit 4step**

"Principle of a balance"

Vin = 4/8 - 1/2 = 9
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Testing time of SAR ADC

- High resolution (10bit)
- Low sampling speed (1MS/s)
- DC linearity testing time
  10 bit → 1024 LSBs
  10 points / 1LSB
  10240 points x 1us = 10 msec
  90 msec

1$ chip → 1sec testing time is reasonable.
Mass volume → Even 1msec testing time reduction is significant cost reduction.
Fast testing of SAR ADC DC linearity

- DC linearity is the important testing item.
- Testing time reduction → cost reduction

- The number of SAR conversion steps reduction during DC linearity testing.
Operation of SAR ADC with BIST

Normal operation
4bit 4step

Test mode operation
4bit 2step

Unknown
Vin

Signal measurement

Adjusting Vref

known
(provided by ATE)

2 step reduction

ADC test

Vin

Unknown
SAR ADC Implementation with BIST

Normal weight data

Timing generator

Address

ROM(normal)

SAR logic

ROM(test)

MUX

out

1

SEL

Digital controller

BIST for faster DC linearity testing

Normal mode

Analog input

Unknown

S/H

MUX

Reg

Digital output

Initial reference voltage level

Initial

reference

voltage

level

SAR ADC Implementation with BIST

Normal weight data

Timing generator

Address

ROM(normal)

SAR logic

ROM(test)

MUX

out

1

SEL

Digital controller

BIST for faster DC linearity testing

Normal mode

Analog input

Unknown

S/H

MUX

Reg

Digital output

Initial reference voltage level

Initial

reference

voltage

level
SAR ADC Implementation with BIST

BIST for faster DC linearity testing

Normal weight data

SAR logic

ROM(normal)  ROM(test)

MUX

address

Digital controller

Timing generator

address

ROM

Testing mode

Ramp input from ATE

Analog input

S/H

MUX

Reg

Digital output

Digital controller

Known

Initial reference voltage level

Internal reference voltage level

Testing mode

SAR logic

ROM

MUX

Reg

Digital output

Digital controller

Known

Initial reference voltage level

Testing mode

SAR logic

ROM

MUX

Reg

Digital output

Digital controller

Known

Initial reference voltage level

Testing mode

SAR logic

ROM

MUX

Reg

Digital output

Digital controller

Known

Initial reference voltage level

Testing mode

SAR logic

ROM

MUX

Reg

Digital output

Digital controller

Known

Initial reference voltage level
Measurement results of 10bit SAR ADC chip

10 steps normal binary operation

5 steps testing mode operation

Results are equivalent.
The basic concept is validated.
Testing time reduction

• Time of setup, settling : 10 msec

Normal

90msec

SAR steps

Proposed testing

53msec

Sampling

• Data transfer and processing : 10 msec

Conventional : 110 msec

Proposed : 73 msec

33% reduction
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Problem of binary search algorithm

4bit 4step
No redundancy

Search result has error.
Digital output has error.
Non-binary search algorithm

- Redundancy
- Correction
- Error

4bit 5step

1step redundancy
Principle of error correction

Expression of “9”

Binary search algorithm

Comparator output: 1 0 0 1 1
Dout = 8 + 4 – 2 – 1 + 0.5 – 0.5 = 9

Non-binary search algorithm

Comparator output: 1 0 1 0 1
Dout = 8 + 3 – 2 + 1 – 1 + 0.5 – 0.5 = 9

Comparator output: 0 1 1 1 1
Dout = 8 – 3 + 2 + 1 + 1 + 0.5 – 0.5 = 9

No error correction

Only one

error correction

Multiple
Comparator-error tolerance testing in non-binary SAR ADC

- In a non-binary SAR ADC, this comparator-error tolerance testing is difficult.

- Proposed simple BIST can check comparator-error tolerance.

- Output patterns are multiple.

  Expression of “9”

<table>
<thead>
<tr>
<th>Error Pattern</th>
<th>Description</th>
<th>Result</th>
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</thead>
<tbody>
<tr>
<td>01111</td>
<td>Comparator error path</td>
<td>Not controllable</td>
</tr>
<tr>
<td>10101</td>
<td>Correct path</td>
<td></td>
</tr>
</tbody>
</table>

Not controllable.
Non-binary SAR ADC with BIST

BIST for non-binary SAR ADC

- Analog input
- S/H
- DAC
- MUX4
- SEL
- MUX2
- Reg
- SAR logic
- ROM
- Digital output

ATE

Digital controller

- Small additional digital circuitry.
- ATE provides digital controller functions.
Non-binary SAR ADC with BIST

BIST for non-binary SAR ADC

- Non-binary weight data
- SAR logic
- ROM
- MUX4
- MUX2
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- Digital output

Analog input

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Non-binary SAR ADC with BIST

BIST for non-binary SAR ADC

Non-binary weight data

SAR logic

ROM

MUX2

Reg

Digital output

Analog input

S/H

DAC

MUX4

1

2

3

0

SEL

Digital controller

ATE

• Small additional digital circuitry.
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Non-binary SAR ADC with BIST

- Small additional digital circuitry.
- ATE provides digital controller functions.
Operation of BIST to test error-tolerance in non-binary SAR ADC

Vin = 8.5
DAC = 8.0

From ATE

<table>
<thead>
<tr>
<th>Step</th>
<th>step2</th>
<th>step3</th>
<th>step4</th>
<th>step5</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
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</table>

Checking upper path
Operation of BIST to test error-tolerance in non-binary SAR ADC

Step 1

Vin = 8.5
DAC = 8.0

1 or 2

From ATE

Checking upper path

Checking lower path
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Conclusion

We have proposed BIST for testing SAR ADCs.

• SAR ADC DC linearity testing time reduction.
  Measurement results validate the basic concept.

• Comparator-error tolerance check BIST in non-binary SAR ADCs.
  Small additional circuitry in cooperation with ATE.