Spread-Spectrum Clocking
in Switching Regulators to Reduce EMI

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- Research Background and Goal
- Principle of DC-DC Converters
- Proposal of Noise Power Spectrum Spread Method in DC-DC Converters
- Implementation and Measurement Results
- Summary
Contents

Research Background and Goal

Principle of DC-DC Converters

Proposal of Noise Power Spectrum Spread Method in DC-DC Converters

Implementation and Measurement Results

Summary
Mobile equipment prevails everywhere
- Mobile phone, Digital still camera, PDA

- Small size, High efficiency
- Multiple supply voltages
- Low-voltage supply
Features of Switching Regulator

- **Merit**
  - High efficiency
  - Continuously varying output voltage
  - Large output current

- **Demerit**
  - Coil is required. bulky and costly
  - Switching noise
We focus on a big problem of switching regulator:

“Switching and harmonic noises”

Proposal of EMI reduction technique

by spreading noise power spectrum
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Principle of DC-DC Converter(1)

In case Clk=ON

\[ \Delta I_{L1} = \frac{V_{dd} - V_{out}}{L} \times T_{on} \]

In case Clk=OFF

\[ \Delta I_{L2} = -\frac{V_{out}}{L} \times T_{off} \]

\[ V_{out} = \frac{T_{on}}{T} \cdot V_{dd} \]

\[ \Delta I_{L1} =\Delta I_{L2} \]

\( T; \) clock period

Output voltage \( V_{out} \) is determined by the clock duty.
Principle of DC-DC Converter (2)

- **Vdd**: Input voltage
- **CLK**: Switching clock
- **L, C**: Low pass filter for smoothing
- **Vout**: Output voltage

![Diagram of DC-DC Converter]

**Switching clock**:

- **Input voltage**: 10V
- **L, C**: Low pass filter
- **CLK**: Switching clock

**Output voltages** for different DUTY cycles:

- **DUTY=25%**: OUT = 2.5V
- **DUTY=50%**: OUT = 5V
- **DUTY=75%**: OUT = 7.5V
DC-DC Converter with PWM Controller

Comparator output
Error amplifier output
Triangular wave
**Features of PWM Control**

**Advantage**
- ON/OFF switching
- High efficiency
- Negative feedback control
- Output is stable regardless of output load.

**Disadvantage**
- Synchronization with clock

![Diagram of PWM Control System]

- Output voltage setting
- PWM
- Switching Regulator
- Load
- Output voltage

**Disadvantage**
- Harmonic noises in specific frequencies
EMI and Switching Regulator

Shield is required to meet EMI Regulations

Proposal of EMI reduction circuit
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Proposed Method

Conventional DC-DC Converter +
Extra Digital Control Circuit

Generated switching noise power spectrum are in specific frequencies.

By spreading the spectrum of switching noise power,
EMI reduction is realized.
Principle of Pseudo-Random Digital Modulation (PRM)

- **Driving Clock**
- **Regulator Output**

- **Normal Clock**
- **PRM Clock**

**Phase Modulation**

- Effect of \( V = L \frac{di}{dt} \)
- Switching Control with Pulse

**Switching Noise**

- Large Switching Noises
- Large Harmonic Noises

**Pseudo-Random Spread Spectrum of Noise Power**
PRM Circuit Implementation

- 3bit LFSR case -

Reset

Input

Clock

Shift Register

LFSR

MUX

SEL1

SEL2

SEL3

in1

in2

in3

in4

in5

in6

in7

Output
3bit LFSR case

Time [μs]
DC-DC Converter with PRM

Proposed PRM Circuit

Reset
PRM input
Clock

PWM Controller

Control Circuit
Conventional Circuit
(No need for modification)
Optimal Clock Phase Shift (1)

- When clock phase shift is too large, output ripple becomes too large.
- When clock phase shift is too small, noise spectrum are not spread sufficiently.

Optimal phase shift is obtained by measurement.
Optimal value of maximum phase shift ($T_{\text{shift}}$)

$$T_{\text{shift}} = \frac{T_{\text{pwm}}}{2}$$

$T_{\text{pwm}}$ = PWM clock period
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Technology: FLEX10K30EQC208 – 3 (Altera)

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<th>Item</th>
<th>Spec.</th>
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<tbody>
<tr>
<td>Spectrum Spread Method</td>
<td>Direct</td>
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<tr>
<td>Shift Register Clock</td>
<td>6MHz</td>
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<tr>
<td>PWM Input</td>
<td>187kHz</td>
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<tr>
<td>PN—code Control Clock</td>
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<td>Supply Voltage</td>
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<td>M-Sequence</td>
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<td>The Number of DFFs</td>
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Measurement Setup
Measured Power Spectrum of Driving Clock

Power spectrum of normal clock (Conventional)

Power spectrum of PRM output clock with 5bit M-sequencer (Proposed)

Maximum peak reduction by 12.7dBm
Input voltage $V_{dd}=3.3\,\text{V}$,  
Clock duty = 50%

Amplitude [V]

Output waveform with normal clock
(Conventional)

Output waveform with PRM clock.
(Proposed)
**Measured Output Power Spectrum of DC-DC Converter**

**Output power spectrum with normal clock (Conventional)**

**Output power spectrum with PRM clock (Proposed)**

*Maximum peak reduction by 12.3 dBm*
Match to the theoretical output voltage.

The proposed method does not affect the (average) output voltage.
The proposed method does not affect efficiency.
Peak Noise Power Spectrum vs. the Number of M-Sequencer Bits

Maximum Noise Power [dBm]

Peak Noise Power Spectrum of Driving Clock

Peak Noise Power Spectrum of Switching Regulator Output

5-bit and 6-bit are reasonable trade-off.
**Summary**

- **Proposal of Noise Power Spectrum Spread Technique**
  - Addition of simple digital circuitry can realize EMI reduction.
    - Low cost, Low power
    - Robust against temperature variation, aging
  - No need for modification of the other parts.
  - Applicable also for voltage-boosting converter.

- **Implementation with FPGA**
- **Confirmation of its effectiveness by measurements**

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<tbody>
<tr>
<td>Max. Peak</td>
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<tr>
<td>Fundamental</td>
<td>5.7dBm</td>
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<td>2nd-harmonics</td>
<td>15.6dBm</td>
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<tr>
<td>3rd-harmonics</td>
<td>12.8dBm</td>
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