Second-Order $\Delta\Sigma$AD Modulator with Novel Feedforward Architecture

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Abstract—This paper proposes novel feedforward architecture of a second-order $\Delta\Sigma$AD modulator with single DAC-feedback topology. $\Delta\Sigma$AD modulator realizes high resolution by oversampling and noise shaping technique. However, its SNDR (Signal to Noise and Distortion Ratio) is limited by the dynamic range of the input signal and non-idealities of building blocks, particularly by the harmonic distortion in amplifier circuits. Compared with a feedbacked $\Delta\Sigma$AD modulator, in a full feedforward $\Delta\Sigma$AD modulator structure, the signal transfer function is unity under ideal circumstances. It means that the signal swings through the loop filter become smaller. Therefore, the harmonic distortion generated inside the loop filter can be significantly reduced because the effect of non-idealities in amplifiers can be suppressed when signal swing is small. Moreover, the reduction of the internal signal swings also relaxes output swing requirement for amplifiers in low-voltage design. However, in conventional feedforward $\Delta\Sigma$AD modulator, an analog adder is needed before quantizer. Especially in a multibit modulator, an additional amplifier is necessary to realize the summation of feedforward signals, which leads to large chip area and extra power dissipation. In this paper, we propose a novel architecture of a feedforward $\Delta\Sigma$AD modulator. It realizes the summation of feedforward signals without additional amplifier that is equivalent to the conventional one but smaller chip area and low-power dissipation. We also conducted MATLAB and SPICE simulations to verify the proposed architecture and modulator circuits.

I. INTRODUCTION

As an interface between the analog world and the digital domain, the ADC (Analog-to-Digital Converter) is widely used in the mixed-signal circuits. However, in deep-submicron CMOS technology, the decrease of the supply voltage evidently degrades the accuracy of ADC. $\Delta\Sigma$AD modulators realize high resolution by oversampling and noise shaping technique, which are the most suitable for high resolution application in the deep-submicron CMOS technology. The performance of $\Delta\Sigma$AD modulators is limited by dynamic range of input signal and non-idealities of building blocks. In nano-meter CMOS technology, the performance of analog circuits is greatly degraded because the devices mismatch grows much with scaling down. Therefore, non-idealities of building blocks, especially non-linearities of amplifiers generate more harmonic distortion. Furthermore, since signal swings are reduced due to lower supply voltage, the dynamic range will be decreased for the same noise floor, and the performance of the modulator is degraded. Circuit level challenge for high resolution with low-voltage operation is limited in the nano-meter CMOS technology. The best solution for the problems is at system level. By applying direct feedforward of input signal to a quantizer, the signal swings in the modulator are significantly reduced. Hence the drawbacks of $\Delta\Sigma$AD modulators can be overcome.

II. FEEDBACK & FEEDFORWARD $\Delta\Sigma$AD MODULATORS

Figs.1 and 2 show second-order feedback and feedforward $\Delta\Sigma$AD modulators respectively. They have similar structure with two integrators, ADC and DAC, but their signal paths are different.

• Feedback $\Delta\Sigma$AD modulator

The input and output of the feedback $\Delta\Sigma$AD modulator shown in Fig.1 can be expressed as

$$Y(z) = z^{-2}X(z) + (1 - z^{-1})^2 E(z)$$ (1)

Here $X(z)$ is input signal, $Y(z)$ is output signal and $E(z)$ is quantization noise of the modulator. Then the signal transfer function ($STF$) and noise transfer function ($NTF$) of the modulator are given by

$$STF(z) = z^{-2}$$ (2)
$$NTF(z) = (1 - z^{-1})^2.$$ (3)

The NTF provides a second-order noise-shaping function for the quantization noise of the modulator. The feedback architecture is the most commonly used topology to $\Delta\Sigma$AD modulators. The output signals of the first and second integrators, $y_1$ and $y_2$ are as follows:

$$y_1 = z^{-1}(1 - z^{-1})X(z) - z^{-1}(1 - z^{-1})E(z)$$ (4)
$$y_2 = z^{-2}X(z) - z^{-1}(2 - z^{-1})E(z)$$ (5)

From Eqs.(4) and (5), we see that the output signals of two integrators $y_1$ and $y_2$ are the functions of $X(z)$, the input signal to the modulator. Then the signal swing at the output of amplifiers becoming large which makes their implementation in the low-voltage more difficult. The harmonics generated by the amplifier non-linearities also depends on the signal swing of integrator, which severely reduces the SNDR of the modulator with feedback topology.
III. PROPOSED NOVEL FEEDFORWARD ΔΣAD MODULATOR ARCHITECTURE

Note the summation point of feedforward paths in front of the quantizer in Fig.1(b), an adder circuit is necessary to realize all the feedforward signals summed together, which creates complication for full feedforward ΔΣAD modulators. In some implementations, this adder is realized by passive switched-capacitor network. However, this approach reduces the signal level into the quantizer and it is only suitable for single-bit implementation. In a multibit implementation of the full feedforward ΔΣAD modulators, the switched-capacitor adder is used and a weighted summation amplifier is required before the quantizer [3], that leads to increased circuit complexity, large chip area and extra power dissipation [4], [5]. Some ideas have been proposed to solve this problem. However, they require a distributed DAC-feedback [4] or high-order(≥3rd-order) loop filter [4], [5]; which significantly increases the complexity of the analog circuit to implement the modulator. We propose here a novel architecture of feedforward ΔΣAD modulators. It is a single DAC-feedback, second-order ΔΣAD modulator without an additional amplifier. Circuits' complexity is reduced and it is more suitable for low-power applications.

Fig.3 shows the proposed architecture of feedforward ΔΣAD modulator. It is a 3-bit second-order structure with single-loop single-DAC-feedback topology. To get higher SNDR with low-power dissipation, proposed modulator has following features:

- **One amplifier saving**
  Compared with the conventional feedforward modulators shown in Fig.2, in our proposed novel architecture, we moved the summation point of feedforward path from input node of quantizer to the input node of the second-stage loop filter. The feedforward signals can be merged into the output of the first integrator, then fed to the second stage. By this way, the amplifier in second stage can be shared to realize signal summation and integration. Therefore, circuits' complexity is reduced by not requiring an additional weighted summation amplifier before the quantizer.

- **Lower-order loop filter and multibit architecture**
  Second-order loop filter reduces the complexity of the analog circuit and power dissipation. Multibit quantizer not only reduces quantization noise, but also relaxes the required slew rate of input amplifier of the filter. Therefore, the modulator becomes more linear, stability is improved and power dissipation is lower also [6].

- **Single DAC-feedback and single-loop topology**
  Furthermore, with a single DAC-feedback, a single-loop topology, rather than a distributed DAC-feedback [7], a cascaded architecture [8], the complexity of the analog circuit and DAC linearization in the ΔΣ modulator is reduced, and modulator is much less sensitive to the finite dc gains of the amplifiers. They are more suitable for low-power dissipation.

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\[ Y(z) = X(z) + (1 - z^{-1})^2 E(z) \]  
\[ STF(z) = 1 \]  
\[ NTF(z) = (1 - z^{-1})^2. \]  

Through Eqs.(9) and (10), we see that the output signals of two integrators \( y_1 \) and \( y_2 \) are free of the input signal \( X(z) \), which means that the feedforward ΔΣAD modulator processes quantization error only [1], [2]. Therefore, the signal swings passing through the integrator are smaller and the distortion generated by the non-linearities effect of the amplifiers is input signal independent. It can be significantly reduced. Furthermore, in this topology, the signal amplitude of the amplifiers is reduced and that eases implementation of amplifier design. Hence, it is more suitable for low-power applications.
From Eqs.(11) and (12), we see that the output signal of first 
\[ \Delta \Sigma \]
the output spectrum of a feedforward 
at the output of the feedback 
of amplifiers cause large harmonic distortion and it appears 
harmonic distortion. It is clear that the gain non-linearities 
modulator in Fig.1 including a nonlinear amplifier model with 
parasitic-incentive implementation of the proposed feedforward 
torus with loop filters and feedback DACs. Parasitic-incentive 
implementation of the proposed feedforward 
coefficient are used, but it is clear that in our proposed 
feedforward modulator, the harmonic distortion is greatly 
coefficients are realized by 
circuit. Feedforward signals are summed at input node of the 
second stage integrator, and no more additional summation 
amplifier is necessary. The coefficients in Fig.3 are realized by 
the ratios of capacitors around the amplifier. In our proposed 
modulator, all coefficients are 1 which are easily implemented 
with the same capacitor size. Nine-level DAC are implemented 
by 8 capacitors which unit size is 1/8 of the input sampling 
capacitor. Therefore, the size of all capacitors can match well.

IV. SIMULATION RESULTS AND CONCLUSION

We have conducted MATLAB and SPICE simulations to 
verify the proposed architecture and the modulator circuits. 
Matlab behavioral model is shown in Fig.3 and SPICE behav-
ioral circuit is shown in Fig.6.

In SPICE simulation, ideal amplifiers and switches are used. 
The values of capacitors are shown in Fig.6. We assume 
that supply voltage is \( V_{dd} = 1.8V \), reference voltages are \( V_{refp} = 1.8V \), \( V_{cm} = 0.9V \) and \( V_{refm} = 0V \), input signals 
are differential sine waves that \( V_{pp} = 1.0V \) and offset at 
0.9V. Fig.7 shows SPICE simulation results of two integrators’ 
output waveform respectively. The output voltage of both 
integrators is in a range of 0 to \( V_{dd} \), which means that the 
two amplifiers work well without any saturation. Especially, 
the output voltage swing of the first integrator is very small; 
it eventually reduces the power consumption and simply eases 
the amplifier design in a low voltage. We also made the 
simulation results comparison between MATLAB and SPICE. 
Fig.8 shows compared simulation results of output spectrum, 
and Fig.9 shows compared results of SNDR-OSR. The SPICE 
behavioral results are similar to MATLAB simulated results. 
It suggests that the proposed circuit realizes the noise shaping 
as well as proposed at system level.

As a result, we have proposed novel feedforward architecture 
and its implementation circuits of a second-order \( \Delta \Sigma \)AD 
modulator. In our proposed novel architecture, an amplifier can 
be shared so that the circuits’ complexity can be reduced. It 
suggests small chip area and low-power dissipation. MATLAB 
and SPICE simulations results show the efficiency of proposed 
architecture and modulator circuits.
Fig. 6. Switched-Capacitor implementation of proposed feedforward $\Delta \Sigma$AD modulator.

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REFERENCES


