A Noise-Shaping Algorithm of Multi-bit DAC Nonlinearities in Complex Bandpass $\Delta\Sigma$ Modulators

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SUMMARY This paper presents a technique for improving the SNR and resolution of complex bandpass $\Delta\Sigma$ADCs which are used for wireless communication systems such as cellular phone, wireless LAN and Bluetooth. Oversampling and noise-shaping are used to achieve high accuracy of a $\Delta\Sigma$AD modulator. However when a multi-bit internal DAC is used inside a modulator, nonlinearities of the DAC are not noise-shaped and the SNR of the $\Delta\Sigma$ADC degrades. For the conversion of complex intermediate frequency (IF) input signals, a complex bandpass $\Delta\Sigma$AD modulator can provide superior performance to a pair of real bandpass $\Delta\Sigma$AD modulators of the same order. This paper proposes a new noise-shaping algorithm—implemented by adding simple digital circuitry—to reduce the effects of the same order. We have performed simulations with MATLAB to verify the effectiveness of the algorithm, and the results show that the proposed algorithm can improve the SNR of a complex bandpass $\Delta\Sigma$ADC with nonlinear internal multi-bit DACs.

key words: complex bandpass $\Delta\Sigma$ modulator, bandpass filter, noise-shaping, ADC, DAC, element rotation, data-weighted averaging, low-IF receiver

1. Introduction

Recently, research into bandpass $\Delta\Sigma$ADCs has become popular for their applications to RF receivers in wireless communication systems such as cellular phone, wireless LAN and Bluetooth [1]–[5]. Shifting the ADC towards the antenna side in the receiver architecture relaxes the requirements placed on analog circuits at the expense of more complicated digital circuit, allowing more digital integration of analog function on a single chip, and resulting in a cheaper system with a higher level of integration. However, ADCs with high linearity, large dynamic range, bandwidth and strong image rejection capabilities are required, and a complex bandpass $\Delta\Sigma$ADC is one of their candidates.

In communication systems applications using complex intermediate frequency (IF) input signals, image signals caused by mismatches between I and Q paths may adversely affect system performance, and a complex bandpass $\Delta\Sigma$AD modulator [1]–[6] can provide better suppression of image signals and thus superior performance to a pair of real bandpass $\Delta\Sigma$AD modulators of the same order. Also especially in low-IF receivers, it is known [3] that the complex bandpass $\Delta\Sigma$AD modulator relaxes the performance requirement (such as sampling speed) over a pair of real bandpass $\Delta\Sigma$AD modulators.

In $\Delta\Sigma$AD modulators, oversampling and noise shaping techniques are used to achieve high accuracy. When a single-bit modulator (i.e., internal ADC and DAC are 1-bit) is used to achieve high SNR, higher oversampling ratio (OSR) is needed which demands higher sampling rate, and/or a high-order filter inside a modulator (as well as a high-order digital filter following the $\Delta\Sigma$AD modulator) is required which may cause modulator stability problems. On the other hand, when a multi-bit $\Delta\Sigma$ modulator is used, higher resolution can be achieved with lower OSR, and the stability problems are alleviated [7], [8].

A multi-bit DAC cannot be made perfect linear, while a 1-bit DAC is inherently linear. Multi-bit $\Delta\Sigma$ nonlinearity is equivalent to errors added directly to the input signal - it is not reduced by noise-shaping, and hence they may degrade the SNR of the $\Delta\Sigma$ADC. The input and output of a bandpass $\Delta\Sigma$AD modulator shown in Fig. 1 are given by

$$M(z) = \frac{H(z)}{1 + H(z)} \left[ X(z) + \frac{1}{H(z)} E(z) + \frac{1}{H(z)} \delta(z) \right]$$

$$Y(z) = \frac{H(z)}{1 + H(z)} \left[ X(z) + \frac{1}{H(z)} E(z) - \delta(z) \right]$$

Here the signal part $S(z)$ and the noise part $N(z)$ are defined as:

$$S(z) := \frac{H(z)}{1 + H(z)} X(z)$$

$$N(z) := \frac{1}{H(z)} \left[ \frac{1}{H(z)} E(z) - \delta(z) \right]$$

From Eq. (3), we see that nonlinearity errors $\delta(z)$ of DAC directly appears at output of the modulator without noise-shaping, while internal quantization noise $E(z)$ of ADC is noise-shaped by $1/H(z)$; this makes it difficult to realize a high resolution ADC.

One way to overcome this multi-bit $\Delta\Sigma$ nonlinearity problem is (self-)calibration of the multibit DAC, and another way is to use signal processing algorithms to noise-shape the multi-bit $\Delta\Sigma$ nonlinearities. There are already some algorithms for noise-shaping of multi-bit DAC nonlinearities in bandpass $\Delta\Sigma$AD modulators, such as dynamic element matching (DEM) [8] and element rotation (data-weighted averaging) [9]. However either of them is for real bandpass $\Delta\Sigma$AD modulators (single-input & output only).
shown in Fig. 1. This paper presents a new algorithm which noise-shapes nonlinearities of multi-bit DACs in a complex bandpass ΔΣAD modulator which has I, Q inputs and outputs. Adding simple digital circuitry can provide first-order complex bandpass noise-shaping of nonlinearities of multi-bit DACs, and improve the SNR of a multi-bit complex bandpass ΔΣADC. Our simulation results with MATLAB show the proposed method can improve the SNR and resolution of complex bandpass ΔΣADCs.

Section 2 reviews DAC nonlinearity noise-shaping algorithms (element rotation methods) for lowpass and highpass modulators with single-input & output, based on [9], [12]. Section 3 describes our proposed DAC nonlinearity noise-shaping algorithm for complex bandpass modulators, and Sect. 4 shows its MATLAB simulation results. Finally Sect. 5 provides conclusion.

Throughout this paper, we assume, without loss of generality, that internal DACs in ΔΣAD modulators have 9-level resolution; their digital input takes the value of 0, 1, 2, ..., 7, or 8. We also suppose that they are implemented with the segmented current-steering DAC architecture [14].

2. DAC Nonlinearity Noise-Shaping Algorithms in Lowpass and Highpass Modulators

In this section, we will describe element rotation (data-weighted averaging: DWA) first-order noise-shaping algorithms of DAC nonlinearities in (single-input & output) lowpass and highpass modulators [9], [12], which will be used for the algorithm derivation for complex bandpass modulators in Sect. 3.

2.1 Normal Segmented DAC and Unit Cell Mismatches

A normal segmented current-steering DAC with 9-level resolution in Fig. 2 consists of 8 unit-current-cells and a resistor. We denote $I_k$ for the current of $k$-th unit-current-cell ($k = 0, 1, 2, \ldots, 7$). Ideally all currents $I_k$ ($k = 0, 1, 2, \ldots, 7$) should be equal, however in practice they can be slightly different due to such as process variation inside an IC chip. Let

$$I_k := I + e_k \quad (k = 0, 1, 2, \ldots, 7).$$

Fig. 2 A current-steering segmented DAC with 9-level resolution. Here $e_0, e_1, \ldots, e_7$ denote current source mismatches.

Fig. 3 (a) Lowpass element rotation architecture. (b) Equivalent block diagram.

Here

$$I := (I_0 + I_1 + I_2 + \ldots + I_7)/8,$$

and $e_k$ is the current mismatch part of $I_k$. When the digital input data is $m$, unit-current-cells of $0, 1, 2, \ldots m - 1$ are ON in any sample time, and the output voltage $V_{out}$ is given by

$$V_{out} = mRI + \delta.$$

Here $\delta$ is DAC nonlinearity given by

$$\delta := R(e_0 + e_1 + e_2 + \ldots + e_{m-1}).$$

In this case the mismatch effects of $e_0, e_1, \ldots, e_7$ (or equivalently DAC nonlinearity $\delta$) to the ADC output cause almost flat power spectrum in the entire band.

2.2 Lowpass Element Rotation

This subsection explains a lowpass element rotation algorithm [12]. Let us consider a circuit in Fig. 3, which consists of a digital lowpass filter $(1/(1 - z^{-1}))$, a DAC with nonlinearity of $\delta(z)$ and an analog high pass filter $(1 - z^{-1})$. Then we have the followings:

$$C_2(z) = \frac{1}{1 - z^{-1}} C_1(z)$$
$$C_4(z) = (1 - z^{-1}) C_3(z)$$
$$C_3(z) = C_2(z) + \delta(z).$$

Thus the analog output of $C_4(z)$ is given by
If we replace a multi-bit DAC in a lowpass \(\Delta\Sigma\) AD modulator with the circuit in Fig. 3, its DAC nonlinearity is noise-shaped. However, in practice this structure cannot work properly; suppose that \(C_1(n)\) is always a positive number, say 2, then the DAC input \(C_2(n)\) becomes infinite (out-of-DAC-input-range) as \(n\) increases. Then the equivalent implementation (called an element rotation algorithm) has to be considered.

First we modify the segmented current-steering DAC as follows:

- Arrange unit-current-cells of the DAC in a ring form as shown in Fig. 4.
- Let the DAC have a pointer to show which unit-current-cell should be selected next sample time, and let the pointer be \(P(n)\) at time \(n\).

Suppose that we have infinite number of unit-current-cells, and \(C_2(n) = a, C_1(n + 1) = b\) (where \(0 \leq b \leq 8\)). Then the unit-current-cells of 0, 1, \ldots, \(a + b - 1\) in the DAC are ON, and it follows from Eqs. (8) and (10) that

\[
C_3(n + 1) = (a + b)RI
+ R(e_0 + e_1 + e_2 + \ldots + e_{a+b-1}).
\]

Since

\[
C_3(n) = aRI + R(e_0 + e_1 + e_2 + \ldots + e_{a-1}),
\]

the analog output \(C_4(n + 1)\) is given by

\[
C_4(n + 1) = C_3(n + 1) - C_3(n)
= bRI + R(e_{a-1} + e_a + e_{a+1} + \ldots + e_{a+b-1}),
\]

which corresponds that the unit-current-cells of \(a - 1, a, a + 1, \ldots, a + b - 1\) in the DAC are ON. However, there are only 8 unit-current-cells in the actual DAC, and \(a + b - 1\) can be larger than 7. Then for the actual implementation of the above structure in the lowpass element rotation algorithm, the unit-current-cells are arranged in a ring form, and in this case the unit-current-cells of \(\text{mod}8(a-1), \text{mod}8(a), \text{mod}8(a+1), \ldots, \text{mod}8(a+b-1)\) are ON. The rigorous description of the lowpass element rotation algorithm is as follows:

- Suppose that the input data \(C_1(n) = c_n\) (where \(n = 0, 1, 2, 3\ldots\)).
- Turn on \(c_n\) unit-current-cells of \(\text{mod}8(P(n) + 1), \text{mod}8(P(n) + 2), \text{mod}8(P(n) + 3), \ldots, \text{mod}8(P(n) + c_n)\).
- Set the pointer at time \(n + 1\) to \(P(n + 1) = \text{mod}8(P(n) + c_n)\).

Figure 5(a) shows the unit-current-cells in ON state which are filled in black when input data are sequentially given by 4, 3, 2, 5, \ldots. When the input is 4 at time \(n\), unit-current-cells of 0, 1, 2, 3 are ON. When it is 3 at time \(n + 1\), those of 4, 5, 6 are ON, and when it is 2 at time \(n + 2\), those of 7, \((\text{mod}8(8)=0)\) are ON. Also when it is 2 at time \(n + 3\), those of \((\text{mod}8(9)=1), (\text{mod}8(10)=2)\) are ON. By selecting unit-current-cells in this way (i.e., always clockwise), mismatches among unit-current-cells are first-order lowpass noise-shaped [11]-[13]. Figure 5(b) shows the noise-shaping effect by MATLAB simulation. The ADC output power spectrum contributed by DAC nonlinearities in the signal band is flat with a normal segmented current-steering DAC, however it is noise-shaped when this algorithm is incorporated.

\[D_2(z) = \frac{1}{1 + z^{-1}} D_1(z)\]
We see that the DAC nonlinearity $\delta(z)$ is first-order noise-shaped by $1 + z^{-1}$. Note that Eqs. (11), (12), (13) are equivalent to the following:

$$D_2(n + 1) = D_2(n) - D_1(n + 1) \quad (15)$$
$$D_3(n + 1) = D_3(n + 1) + D_3(n) \quad (16)$$
$$D_5(n) = D_5(n) + \delta(n). \quad (17)$$

If we replace a multi-bit DAC in a highpass $\Delta \Sigma$ modulator with the circuit in Fig. 6, its DAC nonlinearity is noise-shaped. However, similarly to the lowpass case, this structure cannot work properly and we have to consider its equivalent implementation (a highpass element rotation algorithm).

We modify the segmented current-steering DAC so that the unit-current-cells are in a ring form and the DAC have a pointer $P(n)$. The rigorous description of the highpass element rotation algorithm is as follows:

- At time $2n$:
  - Suppose that the input data $D_1(2n) = d_{2n}$,
  - Turn on $d_{2n}$ unit-current-cells of $P(2n)$, mod$_8(P(2n) + 1)$, mod$_8(P(2n) + 2)$, ..., mod$_8(P(2n) + d_{2n} - 1)$. In other words, $d_{2n}$ unit-current-cells are selected from $P(2n)$ clockwise.
  - Set the pointer at time $2n + 1$ to $P(2n + 1) = \text{mod}_8(P(2n) + d_{2n} - 1)$.

- At time $2n + 1$:
  - Suppose that the input data $D_1(2n + 1) = d_{2n+1}$.
  - Turn on $d_{2n+1}$ unit-current-cells of $P(2n + 1)$, mod$_8(P(2n + 1) + 1)$, mod$_8(P(2n + 1) - 1)$, mod$_8(P(2n + 1) - 2)$, ..., mod$_8(P(2n + 1) - d_{2n} + 1)$. In other words, $d_{2n+1}$ unit-current-cells are selected from $P(2n+1)$ counter clockwise.
  - Set the pointer at time $2n + 2$ to $P(2n + 2) = \text{mod}_8(P(2n + 1) - d_{2n+1} + 1)$.

Figure 7(a) shows the unit-current-cells in ON state while input data are shifted by 4, 3, 2, 6, ... for highpass noise-shaping in element rotation algorithm by $1 + z^{-1}$. When the input is 4 at time $n$, unit-current-cells of 0, 1, 2, 3 are ON. When it is 3 at time $n + 1$, those of 3, 2, 1 are ON, and when it is 2 at time $n + 2$, those of 1, 2 are ON. Also when it is 6 at time $n + 3$, those of 2, 1, 0, 7, 6, 5 are ON. In other words, unit-current-cells are selected clockwise or counter clockwise alternately at every sample time.

3. Complex Bandpass Noise-Shaping Algorithm of DAC Nonlinearities

In this section, we will derive an element rotation algorithm in complex bandpass modulators, based on the element rotation algorithms in lowpass and highpass modulators described in Sect. 2.

3.1 Complex Bandpass $\Delta \Sigma$AD Modulator

Figure 8 shows a complex bandpass $\Delta \Sigma$AD modulator, a first-order complex bandpass filter and its gain characteristics. We see that the complex filter has two inputs and outputs, and it consists of a complex bandpass filter, two internal ADCs and DACs. For example, the transfer function of the complex bandpass filter shown in Fig. 8(b) can be written as follows [6]:

$$H(z) = \frac{1}{z - (c + d + je)}$$

where $c$ and $d$ are design parameters (appropriate constants of real values) which characterize the complex bandpass filter. We see in Fig. 8(c) that the gain of the complex bandpass filter is asymmetrical to the axis of $\omega = 0$.

3.2 Proposed Architecture for Complex Bandpass Noise-Shaping of DAC Nonlinearities

We consider here complex bandpass $\Delta \Sigma$AD modulators whose center of passband is at the normalized frequency of $\omega = \pi/2 (1/4$ of the sampling frequency) [1]–[6]. Figure 9 shows our proposed architecture for complex bandpass noise-shaping of DAC nonlinearities. It consists of a digital complex filter at front-end, two DACs, and an analog complex filter at back-end. $I_i$ is the digital output of the ADC in.
We obtain the following equations in Fig. 9:

\[ Y(z) := I_1(z) + jQ_1(z), \]

and the complex output signal of 2-channel DACs which is fed back to the complex filter is given by

\[ M(z) := I_4(z) + jQ_4(z), \]

we obtain the followings in Fig. 9:

\[ I_5(z) + jQ_5(z) = F(z) \cdot Y(z) \]  (18)
\[ I_5(z) + jQ_5(z) = (I_2(z) + jQ_2(z)) + (\delta_1 + j\delta_2) \]  (19)
\[ M(z) = \frac{1}{F(z)} (I_3 + jQ_3). \]  (20)

By substituting Eqs. (18) and (19) to Eq. (20), we have

\[ M(z) = Y(z) + \frac{1}{F(z)} (\delta_1 + j\delta_2). \]  (21)

Note that Eqs. (1) and (2) hold also for the complex bandpass \( \Delta\Sigma \) modulator if we consider \( H(z) \) is a complex filter and \( X(z), Y(z), E(z) \) and \( \delta(z) \) are complex signals. Then by substituting Eq. (21) to Eq. (1) and sorting it, we obtain

\[ N(z) = \frac{H(z)}{1 + H(z)} \cdot \left( \frac{1}{F(z)} E(z) - \frac{1}{F(z)} (\delta_1(z) + j\delta_2(z)) \right). \]  (22)

We see that by comparing Eq. (22) with Eq. (3), not only the (complex) quantization noise \( E(z) \) of 2-channel ADCs is noise-shaped by \( 1/H(z) \), but also the 2-channel DACs (complex) nonlinearities error \( (\delta_1 + j\delta_2) \) is noise-shaped by \( 1/F(z) \).

### 3.3 Realization Algorithm for Proposed Architecture

We obtain the following equations in Fig. 9:

\[ I_2(n + 1) = I_1(n) - Q_2(n) \]  (23)
\[ I_3(n + 1) = I_3(n) + Q_2(n) \]  (24)
\[ I_3(n) = I_3(n) + \delta_1(n) \]  (25)
\[ Q_3(n + 1) = I_3(n) + Q_3(n) \]  (26)
\[ Q_4(n + 1) = Q_3(n + 1) - I_3(n) \]  (27)
\[ Q_4(n) = Q_2(n) + \delta_2(n). \]  (28)

The direct realization of the proposed architecture in Fig. 9 is not possible because \( I_2, Q_3 \) can be out-of-input-range of the following I, Q-channel DACs. For example, suppose that

\[ I_1(n) + jQ_1(n) = \exp(j\frac{\pi}{2} n) + 4. \]

This can happen because the center of the signal band in the modulator is at the normalized frequency of \( \omega = \pi/2 \), and \( I_1, Q_1 \) are integer values between 0 to 8. Then it follows from Eqs. (23) and (26) that

\[ I_2(1) = 5 - Q_2(0), \quad I_2(2) = -I_2(0), \]
\[ I_2(3) = -7 + Q_2(0), \quad I_2(4) = I_2(0) \]
\[ Q_3(1) = 4 + I_2(0), \quad Q_3(2) = 10 - Q_2(0), \]
\[ Q_3(3) = 4 - I_2(0), \quad Q_3(4) = -4 + Q_2(0). \]

We see that \( I_2 \) and \( Q_3 \) can be out of the DAC input range \( (0, 1, 2, \ldots, 8) \).

Now we describe an equivalent realization of the proposed architecture; our implementation use only a digital filter at front-end of 2-channel DACs and does not require an analog filter at back-end.

[ Proposed Algorithm ]

We modify the two segmented current-steering DACs as follows (Fig. 10(a)):
Now we will explain how this algorithm was derived and why it is equivalent to the architecture in Fig. 9.

First, we consider the I-channel. The I-channel DAC (whose output is $I_n$ as shown in the upper part of Fig. 9) is equivalent to [Highpass digital filter + DAC + Lowpass analog filter]; look at the left part of Fig. 6(b) and the upper-left part of Fig. 9, and also compare Eqs. (23) and (15). If $Q_2(n)$ in Eq. (23) is replaced with $I_2(n)$, Eq. (23) has the same form as Eq. (15). Similarly look at the right part of Fig. 6(b) and the upper-right part of Fig. 9, and also compare Eqs. (24) and (16). If $Q_2(n)$ in Eq. (24) is replaced with $I_2(n)$, Eq. (24) has the same form as Eq. (16). Also Eq. (25) has the same form as Eq. (17). Thus we see the following:

- For the I-channel DAC output $I_n$, we apply a highpass element rotation algorithm with internal interaction between I, Q paths.

Next, we consider the Q-channel. The Q-channel DAC (whose output is $Q_n$ as shown in the lower part of Fig. 9) is equivalent to [Lowpass digital filter + DAC + Highpass analog filter]; look at the left part of Fig. 3(b) and the lower-left part of Fig. 9, and also compare Eqs. (26) and (8). If $I_2(n)$ in Eq. (26) is replaced with $Q_2(n)$, Eq. (26) has the same form as Eq. (8). Similarly look at the right part of Fig. 3(b) and the lower-right part of Fig. 9, and also compare Eqs. (27) and (9). $I_2(n)$ in Eq. (27) is replaced with $Q_2(n)$, Eq. (27) has the same form as Eq. (9). Also Eq. (28) has the same form as Eq. (10). Thus we see the following:

- For the Q-channel DAC output $Q_n$, we apply a lowpass element rotation algorithm with internal interaction between I, Q paths.

Now we consider the interactions between I-path and Q-path.
in Fig. 9 (or equivalently in Eqs. (23), (24), (26) and (27)). It follows from Eqs. (23) and (24) that the I-channel output \( I_4 \) at time \( n+1 \) is a function of the Q-channel internal states \( (Q_2(n), Q_3(n)) \) at time \( n \) as well as the I-channel input \( I_1 \). Also we see from Eqs. (26) and (27) that the Q-channel output \( Q_4 \) at time \( n+1 \) is a function of the I-channel internal states \( (I_2(n), I_3(n)) \) at time \( n \) as well as the Q-channel input \( Q_1 \). Noting that the pointers \( P_1(n), P_2(n) \) keep some information of the I, Q channels internal states, we have the following observation:

- If DAC1 with a pointer \( P_1 \) is used for I-channel and DAC2 with a pointer \( P_2 \) is used for Q-channel at time \( 2n \), then DAC1 is used for Q-channel and DAC2 is used for I-channel at time \( 2n+1 \).

Then the proposed algorithm is derived and the nonlinearities of 2-channel DACs, \( \delta_1, \delta_2 \), will be first-order complex bandpass noise-shaped.

4. Simulation of Proposed Algorithm

We have conducted MATLAB simulations to confirm the noise-shaping function on multi-bit DAC nonlinearities of the proposed algorithm. We used a fourth-order complex modulator [15] with internal ADCs/DACs of 9-level resolution in three cases. Figure 11 shows the complex bandpass filter used inside the modulator, where three poles are located at the normalized angular frequency of \( \omega = \pi/2 \) while one is at \( \omega = 3\pi/2 \); the reason that one pole is located at \( \omega = 3\pi/2 \) is that when this complex filter is incorporated in a modulator in Fig. 8, the quantization noise of the modulator is reduced by noise-shaping at \( \omega = 3\pi/2 \), which will appear at \( \omega = \pi/2 \) of the modulator output as image quantization noise caused by I, Q mismatches inside the modulator. For all three cases, the same analog complex bandpass filter and two ideal internal ADCs in a \( \Delta \Sigma \) modulator were used. However two DACs in a modulator in three cases are different as follows:

- Case 1: Two identical and ideal (linear) DACs were used.
- Case 2: Two normal segmented current-steering DACs with mismatches among unit-current-cells were used.
- Case 3: Two DACs whose mismatches are the same as case 2 and which employ the proposed element rotation algorithm were used.

Figures 12, 13 show the simulation result comparison for output spectrum and SNR of modulators in three cases, where the simulation conditions are as follows:

- In cases 2 and 3, \( e_0, e_1, e_2, \ldots, e_7 \) in DAC1 are 0.0023, \(-0.0015, -0.003, 0.0028, 0.0025, 0.0029, -0.001 \) and 0.0 (LSB) while those in DAC2 are \(-0.0017, 0.0015, -0.0025, 0.002, 0.0026, 0.0, -0.0019, \) and 0.0 (LSB).
- 16 K-point FFT is used to obtain the SNR.
- Input frequency \( (f_{in})/\text{sampling frequency } (f_s) = 4,095/16,384 \).

We see that in case 1, SNR of the ADC increases as OSR increases. However in case 2, SNR saturates as OSR increases; for small OSRs, quantization noise is dominant but it is noise-shaped and hence SNR improves as OSR in-
Fig. 14 Simulation results of the modulator SNR versus rms values of mismatches $e_0, e_1, e_2, \ldots, e_7$ for OSR = 32, 64, 128 and 256. The left graph shows in case that normal segmented DACs are used while the right graph shows in that case that our proposed algorithm is incorporated.

Fig. 15 The simulated results of the output power spectrum focused around the signal band in Fig. 12, where $(4,095/16,384) f_s$ is the signal frequency component. (a) Case 1. (b) Case 2. (3) Case 3. We see that in case 2 SNR degrades rapidly as rms value increases while in case 3 SNR is improved.

creases. However for high OSRs the noise due to DAC nonlinearity becomes dominant, which is not noise-shaped and hence increasing OSR does not help much improve SNR. On the other hand, in case 3, the noise caused by nonlinearities of DAC is pushed out from the signal band, and their influence to the ADC accuracy is reduced which leads to the ADC SNR improvement.

Figure 14 shows simulation results of the modulator SNR versus rms values of mismatches $e_0, e_1, e_2, \ldots, e_7$ for OSR = 32, 64, 128 and 256. Here the value of the mismatches is defined by

$$\text{rms} := \sqrt{(e_0^2 + e_1^2 + e_2^2 + \ldots + e_7^2)/8}$$

and the ratios of $e_0, e_1, e_2, \ldots, e_7$ in DAC1 are 0.0023, $-0.0015, -0.003, 0.0028, 0.0025, 0.0029, -0.001$ and 0.0 (LSB) while those in DAC2 are $-0.0017, 0.0015, -0.0025, 0.002, 0.0026, 0.0, -0.0019,$ and 0.0 (LSB). The left graph shows in case 2 while the right graph shows in case 3. We see that in case 2 SNR degrades rapidly as rms value increases while in case 3 SNR is improved.

We observe in Figs. 13, 14 that in case2 SNR does not improve even if OSR increases for relatively large DAC nonlinearities (if the spectrum of the DAC nonlinearities error is white, twice of OSR leads to at least 3 dB SNR improvement, even if it is not noise-shaped); this is because there are spurious tones at the frequencies of $(4,091/16,384) f_s$ and $(4,099/16,384) f_s$ due to large DAC nonlinearities (Fig. 15), which are the main noise (distortion) components and are not removed with this range of OSRs.

5. Concluding Remarks

We have proposed a new noise-shaping algorithm of multi-bit DAC nonlinearities for a high resolution complex bandpass $\Delta\Sigma$ modulator. The performance of the complex bandpass $\Delta\Sigma$ modulator can be improved by adding some simple digital circuits. The effectiveness of proposed algorithm is confirmed by MATLAB simulation. Finally we remark the followings:

- In the proposed algorithm, at time $2n$, DAC1 is used for I-channel and DAC2 is for Q-channel, while, at time $2n + 1$, DAC1 is for Q-channel and DAC2 is for I-channel; DAC1, DAC2 are used alternately for I, Q-channels, and hence the harmful influence by mismatches between 2-channel DACs is expected to be suppressed with this algorithm.
- The proposed algorithm is applicable to multi-bit complex bandpass $\Delta\Sigma$ modulators as well as AD modulators. The importance of the bandpass $\Delta\Sigma$ modulator is described in [16].
- Our approach here is to improve the accuracy of analog circuits using digital signal processing techniques. We believe that such an approach becomes more important, because as the VLSI technology progresses and the device size scales down, the supply voltage goes down, which makes it difficult to achieve the high accuracy of analog circuits with only circuit technique. On the other hand, the digital circuit becomes faster, cheaper and lower power, which makes rather complicated digital signal processing algorithm feasible to utilize for the analog circuit performance improvement.

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