Channel Linearity Mismatch Effects in Time-Interleaved ADC Systems

Naoki KUROSAWA†, Nonmember, Haruo KOBAYASHI[a], Regular Member, and Kensuke KOBAYASHI††, Nonmember

SUMMARY A time-interleaved ADC system is an effective way to implement a high-sampling-rate ADC with relatively slow circuits. In the system, several channel ADCs operate at interleaved sampling times as if they were effectively a single ADC operating at a much higher sampling rate. Mismatches among channel ADCs degrade SNR and SFDR of the ADC system as a whole, and the effects of offset, gain and bandwidth mismatches as well as timing skew of the clocks distributed to the channels have been well investigated. This paper investigates the channel linearity mismatch effects in the time-interleaved ADC system, which are very important in practice but had not been investigated previously. We consider two cases: differential nonlinearity mismatch and integral nonlinearity mismatch cases. Our numerical simulations show distinct features of such mismatch especially in frequency domain. The derived results can be useful for deriving calibration algorithms to compensate for the channel mismatch effects.

key words: ADC, interleave, channel mismatch, DNL, INL

1. Introduction

Electronic devices are continuously getting faster and accordingly the need for instruments such as digitizing oscilloscopes and LSI testers to measure their performance is growing. Analog-to-digital converters (ADCs) incorporated in such instruments have to operate at very high sampling rate [1], [2]. This paper studies the theoretical issues of a time-interleaved ADC system where several channel ADCs operate at interleaved sampling times as if they were effectively a single ADC operating at a much higher sampling rate [3]–[8]. Figure 1 shows such an ADC system where each of \( M \) channel ADCs \((ADC_1, ADC_2, \ldots, ADC_M)\) operates with one of \( M \) phase clocks \((CK_1, CK_2, \ldots, CK_M)\) respectively. The sampling rate of the ADC as a whole is \( M \) times the channel sampling rate. Such a time-interleaved ADC system is an effective way to implement a high-sampling-rate ADC with relatively slow circuits, and is widely used. Ideally characteristics of channel ADCs should be identical and clock skew should be zero. However, in reality there are mismatches such as offset, gain, bandwidth mismatches among channel ADCs as well as timing skew of the clocks distributed to them, which cause so-called pattern noise and significantly degrade SNR (the number of effective bits) and SFDR of the ADC system as a whole. In practice, often calibration is required to ensure uniformity among the characteristics of the channels. It is important to clarify such issues which are involved in the design of time-interleaved ADC systems.

In previous studies, the effects of offset, gain, timing and bandwidth mismatches have been intensively investigated [9]–[14]. In this paper, we will investigate the linearity mismatch effect. The significance and complexity of linearity mismatch in practical applications was pointed out quite recently—during the 13th Workshop on Circuits and Systems at Karuizawa in April 2000—by a practicing engineer who actually designs high-speed data acquisition systems using time-interleaved ADCs.

We will consider two cases (i.e., differential nonlinearity (DNL) mismatch and integral nonlinearity (INL) mismatch cases), and our numerical simulations show interesting results especially in the frequency domain. To the best of our knowledge, this is the first full paper that discusses the linearity mismatch effects [15], [16].

Hereafter, we will use the following notations:
- \( M \): number of channel ADCs in the ADC system,
- \( f_{in} \): input frequency applied to the ADC system,
- \( f_s \): sampling frequency of the ADC system,
2. DNL Mismatch Effects

Suppose that DNLs and INLs of all channel ADCs are less than 0.5LSB and 1LSB respectively, but their DNLs (and also INLs) have mismatches. We will call this case DNL mismatch. Figure 2(a) explains DNL of a nonideal ADC while Fig. 2(b) shows an example of DNL mismatches. Figure 2(d) shows simulated 8-channel interleaved ADC output (Fig. 2(c)) for a sinusoidal input when channel ADCs have DNL mismatches. We observe so-called "1 LSB noise". Figure 2(e) shows simulated power spectrum of 8-channel interleaved ADC output when channel ADCs have DNL mismatches, and there does not appear to be any distinct error power spectrum due to DNL mismatches. However, we will characterize the error power spectrum due to DNL mismatches as the quantization noise power spectrum dis-
For a sinusoidal input, we rearrange the ADC output waveform to reconstruct a waveform of one period using a modulo time plot [17] (which is a similar technique to equivalent-time sampling, see Fig. 3). Since the output is reconstructed as a sine wave of one period, after its DFT, the signal power spectrum has peak at the frequency of the first bin (Fig. 4(a)). Also we observe a power spectrum skirt of quantization noise around the signal power spectrum as shown in Fig. 4(a). We note that the quantization noise of even an ideal ADC is not white for a sinusoidal input and has similar power spectrum to Fig. 4(a); it can be analyzed using Chebysev polynomials [18]. Now let us consider the DNL mismatch case. Figure 4(b) shows simulated power spectrum with DNL mismatches after modulo
Simulation results of SNR versus $f_{in}$ of an 8-bit 8-channel interleaved ADC system with DNL mismatches. SNR of the whole interleaved ADC is almost equal to the average of channel SNRs (just 0.1 dB below).

Fig. 8 (a) Output waveform of a 2-channel interleaved ADC with DNL mismatches for a DC input. (b) Output power spectrum of a 2-channel interleaved ADC with DNL mismatches for a DC input.

Fig. 9 (a) Ideal 8-bit ADC characteristics and INL. (b) INL mismatch example. (c) 8-bit 8-channel interleaved ADC output for a sinusoidal input when its channel ADCs have INL mismatches.

Remark (i) The relationship between the frequency bins of $k$ (before modulo time plot) and $l$ (after modulo time plot) is given as $k = \mod_N(nl)$, where $N$ is the number of output points (DFT points) and $f_{in}/f_s = n/N$. Then for the original signal (i.e., before applying the modulo plot algorithm) the error power peaks due to DNL mismatch are at $k f_s/M \pm n f_{in}$ ($k = 0, 1, 2, \ldots, M - 1; n = 0, 1, 2, 3, \ldots$).
(ii) The fact that the quantization noise for the sinusoidal input is not white even for an ideal ADC, but it has peaks at \( n \)-th order harmonics and they tend to decrease as \( n \) increases can be intuitively interpreted as follows: it is well-known that in general the output power of a slightly nonlinear system for a sinusoidal input has peaks at \( n \)-th order harmonics and they decrease as \( n \) increases. Since the quantization is slightly nonlinear operation if DNL is not large, the similar effect is observed in this case.

(iii) Regarding the total SNR of a time-interleaved ADC with DNL mismatches, our simulation results show that SNR of the whole interleaved ADC is almost equal to (slightly below) the average of channel SNRs (see Fig. 7).

(iv) For a DC input, our simulation shows that
pattern noise whose power spectrum are at $k f_s / M$, $(k = 0, 1, \ldots, M - 1)$ is caused (see Fig.8), and this effect is similar to the offset mismatch case [9], [10].

(v) In this paper we only describe the simulation results for DNL mismatches in Fig.12. However, we have tried extensive simulations for other DNL mismatch cases, and we have found that the same arguments above also hold in these cases.

3. INL Mismatch Effects

Next let us consider the case that channel ADCs have considerable amount of INLs (not necessarily less than 0.5LSB) and also their INLs can be mismatched. We will call this case INL mismatch. Figure 9(a) explains INL of a nonideal ADC while Fig. 9(b) shows an example of INL mismatches. Figure 9(c) shows simulated 8-bit 8-channel interleaved ADC output for a sinusoidal input when its channel ADCs have INL mismatches, where pattern noise is observed. Figures 10(a) and (b) show simulated power spectrum of an 8-bit interleaved ADC output with INL (but without INL mismatches), and we observe harmonic power bands at $k f_{in}$ ($k = 0, 2, 3, \ldots$). On the other hand, Figs. 10(c) and (d) show simulated power spectrum of an 8-bit 8-channel interleaved ADC output with INL mismatches, and we see that error power peaks are at frequencies of $k f_s / 8 \pm n f_{in}$ ($k = 0, 1, 2, 3; n = 0, 1, 2, 3, \ldots$). Figures 10(e) and (f) show 4-channel and 2-channel cases respectively. Note that simulated power spectrum results in Fig.10 are for ADC outputs without modulo time plot processing.

Fig. 11 Simulation results of SNR versus $f_{in}$ of a 8-bit 8-channel interleaved ADC system with INL mismatches. SNR of the whole interleaved ADC is much worse than the average of channel SNRs.

Fig. 12 DNL examples of an 8-bit ADC used for simulation. (a) Channel 1. (b) Channel 2. (c) Channel 3. (d) Channel 4. (e) Channel 5. (f) Channel 6. (g) Channel 7. (h) Channel 8.
channel ADC sampling frequency $f_s/M$.

(ii) Our simulation results for the total SNR of a time-interleaved ADC with INL mismatches show that SNR of the whole ADC is much worse than the average of channel SNRs, but the average of channel SNRs is better than the worst SNR of the channel ADCs (see Fig. 11).

(iii) The fact that the SNR due to the DNL mismatch is almost the average of channel SNRs while that due to INL mismatch is far below their average can be interpreted as follows; in the DNL mismatch case, we assume that DNL and INL are less than 0.5LSB and 1LSB respectively, which results in small nonlinearity. Thus the ADC system can be approximated as a linear system and hence its SNR is almost the average (i.e., superposition is almost valid). On the other hand, in the INL mismatch case, we assume that each channel may have large INL and hence the ADC system is strongly nonlinear and its SNR is much worse than the average.

(iv) DNL mismatch is related to quantization, while INL mismatch is not. INL mismatch is related to interleaved sampling systems, so applies not only to interleaved ADC systems but also to interleaved track/hold circuits (see Fig. 12).

(v) In this paper we only describe the simulation results for INL mismatches in Fig. 13. However, we have tried extensive simulations for other INL mismatch cases, and we have found that the same arguments above hold also in these cases.

4. Conclusion

We have analyzed the channel linearity mismatch effects in the time-interleaved ADC system, which are very important in practice but have not been investigated yet. We considered two cases: INL and DNL mismatch cases. Our numerical simulation showed their distinct features, especially in frequency domain as well as SNR. Finally we note that we are investigating digital compensation algorithms for linearity mismatches in the time-interleaved ADC system to improve its SNR and SFDR as an on-going project.

Acknowledgement

We would like to thank A. Minegishi, T. Komuro, H. Sakayori, and K. Wilkinson for valuable discussions.

References


Haruo Kobayashi received the B.S. and M.S. degrees in information physics from University of Tokyo in 1980 and 1982 respectively, the M.S. degree in electrical engineering from University of California at Los Angeles (UCLA) in 1989, and the Dr. Eng. degree in electrical engineering from Waseda University in 1995. He joined Yokogawa Electric Corp. Tokyo, Japan in 1982, where he was engaged in the research and development related to measuring instruments and mini-supercomputers. From 1994 to 1997 he was involved in research and development relating to ultra-high-speed ADCs and DACs at Teratec Corporation. In 1997 he joined Gunma University and presently is an Associate Professor in Electronic Engineering Department there. He was also an adjunct lecturer at Waseda University from 1994 to 1997. His research interests include analog & digital integrated circuit design and signal processing algorithms. He is a recipient of the 1994 Best Paper Award from the Japanese Neural Network Society.

Kensuke Kobayashi received the B.S. degree in electronic engineering from the University of Tokyo in 1971. In 1971 he joined IWATSU Electric Co. Ltd., where he was engaged in designing wideband sampling oscilloscopes. From 1993 to 2001, he joined Teratec Corporation and developed fast-sampling-rate and wideband data acquisition systems. In 2001 he joined LeCroy Corp. and is involved in ultra wideband oscilloscope research.

Naoki Kurosawa received the B.S. degree in electronic engineering from Gunma University, Japan in 2000, and currently he is an M.S. course student there. His research interests include analog integrated circuit design.